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A 0.18 µm Differential LNA with reduced Power Consumption

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***Abstract*—This work presents the design of an inductively source degenerated CMOS differential common source cascode Low Noise Amplifier (LNA) operating at 2 GHz frequency. An inductor is added at the drain of the main transistor to reduce the noise contribution of the cascode transistors. Another inductor connected at the gate of the cascode transistor and capacitive cross-coupling are strategically combined to reduce the noise and to increase power gain of the cascode transistors in a differential cascode LNA. The proposed design can reduce the power consumption, and increase the power gain of the LNA. The area occupied by the proposed design measured from the layout is observed as 1.111 mm × 1.27 mm. The LNA is designed with the 0.18 µm standard CMOS process. Cadence design tool Spectre_RF is used to design and simulation based on resistors, inductors, capacitors and transistors.**

***Keywords* - Low Noise Amplifier (LNA), CMOS, noise figure (NF), IIP3, capacitive cross-coupling and RF circuit.**

I. INTRODUCTION

The growth of wireless services and other communication applications has increased the demand of low-cost Radio-Frequency Integrated Circuits (RFICs) and pushed the semiconductor industry towards complete system-on-chip solutions. The radio frequency signal received at the antenna normally is weak. Therefore, an amplifier with a high gain and good noise performance is needed to amplify this signal before it can be fed to other parts of the receiver [1]. Such an amplifier is referred to as a Low Noise Amplifier and forms an essential component of any RF integrated circuit receiver. The main effect of the LNA is to amplify the signal which is received by the antenna. It should provide enough gain, low noise figure, high linearity, great input and output matching with restraint of power consumption [2]. A good LNA has a low noise figure (NF), a large enough gain and low power consumption. The total noise performance of the receiver depends on the Gain and Noise Figure of the LNA. The inductively degeneration common source topology is used for very low power consumption.

RF circuits must process analog signals with a wide dynamic range at high frequencies. RF components constitute a very small fraction of the whole chip but consume lot of design time. This is mainly because RF IC design involves a lot of tradeoffs in power, linearity, gain, frequency, and noise. At least any two of six parameters trade with each other to some extent.

Additional inductors can be added at the drain of the main transistor to improve the gain and noise performance of the inductively source degenerated differential LNA. In this work, a noise reduction inductor combined with the capacitive cross-coupling technique is proposed to improve the noise and linearity performance of the inductively source degenerated differential cascode LNA. The LNA has a double-ended input and differential outputs to avoid an external balun for low cost communication. Sections II describes the basic inductively source degenerated LNA, Input impedance matching, Noise figure and capacitor cross-coupled Differential cascode LNA designs are explained. Section III describes the simulation results and wave forms. Section IV describes the conclusion of this paper.

II. NA DESIGN

A. *Source Degenerated LNA*

A source degenerated LNA is depicted in fig. 1. The L_s is the degeneration inductor. We can adjust the inductor to fit the variation of f_T, but f_T = 2 GHz is so large that the value of the inductor will be less than 0.4nH, which is difficult to be implemented on chip [3]. So the capacitor C_x is added between the gate of the MOSFET and source of MOSFET. The small signal equivalent circuit of Source Degenerated LNA is as shown in fig. 2.

Writing Kirchhoff's equations for Source degenerated LNA

$$I_0 = g_m V_{gs} = I_{in} \times \frac{1}{sC_{gs} + sC_x} g_m = \frac{g_m}{sC_{gs} + sC_x} I_{in} \cdots (1)$$

$$V_{in} = \left[s\left(L_g + L_s\right) + \frac{1}{sC'_{gs}} \right] I_{in} + I_0 sL_s \cdots\cdots (2)$$

Where

$$C'_{gs} = C_{gs} + C_x \cdots\cdots (3)$$

Solving (1) and (2)

$$Z_{in} = \frac{V_{in}}{I_{in}} = s\left(L_s + L_g\right) + \frac{1}{sC'_{gs}} + \frac{g_m L_s}{C'_{gs}} \cdots\cdots (4)$$

$$Z_{in}(j\omega) = j\left[\left(L_g + L_s\right)\omega - \frac{1}{\omega C'_{gs}} \right] + \frac{g_m L_s}{C'_{gs}} \cdots\cdots (5)$$

Matching occurs when $Z(j\omega_0) = R_S$. R_S is the resistor, which is associated with the input voltage source.

$$\left(L_g + L_s\right)\omega_0 = \frac{1}{\omega_0 C'_{gs}} \cdots\cdots (6)$$

$$\omega_0^2 = \frac{1}{\left(L_g + L_s\right)C_{gs}^{'}} \cdots\cdots(7)$$

and

$$R_S = \frac{g_m L_s}{C_{gs}^{'}} \cdots\cdots(8)$$

$$L_g = \frac{1}{\omega_0^2 C_{gs}^{'}} - L_S \cdots\cdots(9)$$

and

$$L_S = \frac{1}{\omega_0^2 C_{gs}^{'}} - L_g \cdots\cdots(10)$$

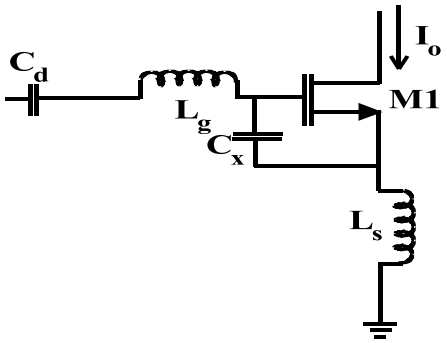

Fig. 1. Source Degenerate LNA

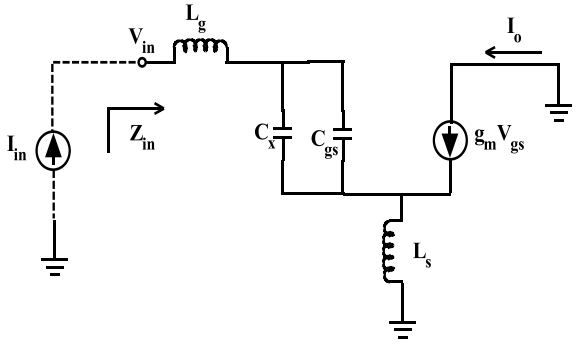

Fig. 2. Small signal equivalent circuit if Source Degenerated LNA.

B. Input impedance matching

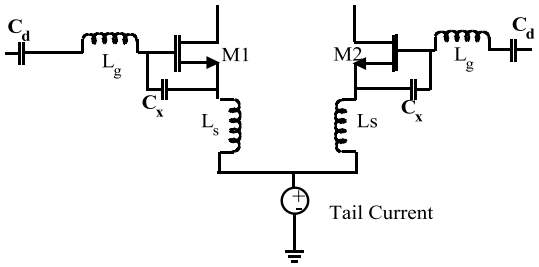

Fig. 3. Input impedance matching

The capacitor C_x is added between the gate of the MOSFET and source of MOSFET as shown in fig. 3. The use of C_x capacitance is to increase the source degenerated inductor value, increase the noise figure, and reduce the power gain of the LNA. The conditions for input impedance matching Z_{in} and the expression for the resonant frequency ω_0 are shown in (11). L_s and L_g together with the capacitance C_{gs} and C_x form an input impedance matching network. The input impedance matching is taken to be 50Ω.

The gate inductance L_g is used to set the resonance once L_s is chosen to satisfy the criterion of a 50Ω pure resistance [4].

$$Z_{in}(s) = \frac{1}{sC_{gs}^{'}} + s\left(L_S + L_g\right) + \frac{g_m}{C_{gs}^{'}} L_S \cdots\cdots(11)$$

$$C_{gs}^{'} = C_{gs} + C_x \cdots\cdots(12)$$

C. Noise Figure

Noise is present in any electrical system and is due to varieties of sources. At higher frequencies, the random movement of electrons is the main source of noise in a system. The fundamental noise performance parameter is the Noise Factor (F), which is defined as the ratio of the total output noise power to the output noise due to input source. If the Noise Factor is expressed in decibels it is called the Noise Figure (NF). It needs higher linearity and sufficient gain. The noise Factor is defined as:

$$NF = 10\log(F) = 10\log\left(\frac{SNR_{in}}{SNR_{out}}\right) \cdots\cdots(13)$$

$$= 10\log\left(\frac{\frac{signal}{noise_{in}}}{\frac{signal}{noise_{out}}}\right) = 10\log\left(1 + \frac{noise_{amp}}{noise_{in}}\right) \cdots\cdots(14)$$

$$F_{total} = F_1 + \frac{F_1 - 1}{G_1} + \frac{F_2 - 1}{G_1 G_2} + \cdots\cdots(15)$$

Where F_n (n=1, 2, 3 ……) is the noise factor of each stage, G_n (n=1, 2, 3 …….) is the gain of each stage.

D. Capacitor cross-coupled Differential cascode LNA design

Differential circuits are of great use in many circuit design topologies because they offer several important advantages over single-ended circuits [5]. The first important advantage is the differential LNA offers a stable reference point. With any type of circuit, the measured values are always taken with respect to a reference. In the differential LNA the measured results of one-half circuit are always taken with respect to other half circuit. Another significant and relevant benefit of using a differential circuit is noise reduction. The inductively source degenerated differential cascode LNA can be considered as a CS-CG two stage LNA.

To supply a differential signal to each LNA input, an "ideal" balun (balanced to unbalanced) transformer has been used (The two AC sources each set to some voltage and opposite polarity can be used). In addition another balun is used on the amplifier output to re-combine the signal to allow

the voltage gain to be simulated. When balun is not used at the output then two ports are required at the output. An additional inductor L_{add} combined with the capacitive cross-coupling technique is applied to the cascode transistors of the differential LNA to reduce the noise and increase the gain. In order to make the differential LNA circuit, two single-ended circuits built, where each transistor and circuit component has a complimentary transistor or component. The positive input voltage is measured at the gate of one of the half-circuit CS amplifiers, while the negative input voltage is measured at the gate of the other half-circuit. The overall output of the LNA is measured between the sources of each half-circuit.

A capacitor cross-coupled differential cascode LNA design circuit shown in fig. 4. Inter-stage inductor with parasitic capacitance form impedance match network between input stage and cascoded stage boost gain, reduce the noise figure and affects the input match condition.

III. SIMULATION

Using the library UMC_18_CMOS for 0.18µm technology in cadence, the schematic of fully capacitor cross-coupled differential cascode LNA on Virtuoso schematic editor tool is created as shown in Fig. 5. We have simulated our design using Cadence spectre_RF tool on UMC 0.18 µm technology. Cadence EDA tools used are Virtuoso for schematic editing and Spectre for simulation.

A. Simulation Results

The various simulation iterations are performed on the capacitor cross-coupled differential cascode LNA circuit to meet design requirements. The simulation results of capacitor cross-coupled differential cascode LNA and the simulation results of post layout capacitor cross-coupled differential cascode LNA operating at 2GHz operating frequency and supply voltages are 1.5 V and 1.8 V. We obtained various results which achieved at the typical process and comparison of resistor. Accordingly in order to meet noise figure, power gain and voltage gain, we have adjusted the sizes of transistors, inductors and resistors. To achieve required values for S_{11} and S_{22}, we have adjusted the sizes of inductors and capacitors. DC analysis is used to calculate power consumption; scattering parameter analysis is used to calculate the noise figure, power gain, S_{11} and S_{22}. For calculating IIP3, 1dB compression point, voltage gain and noise we can use periodic steady state analysis and periodic noise analysis. Fig. 7, fig. 8, fig. 9, fig. 10, fig. 11 and fig. 12 shows the noise figure, power gain, voltage gain, S_{11}, S_{22} and IIP3 operating at 2GHz frequency and supply voltage is 1.8 V. The voltage gain is 16.957 dB, power gain is 21.42 dB, S_{11} is -6.612 dB, noise figure (NF_{min}) is 2.049 dB and IIP3 is -19.05 dBm obtained by simulation. The layout of capacitor cross-coupled differential cascode LNA design circuit is depicted in fig. 6.

this LNA with the published literature is summarized in the Table I.

B. Simulation Wave forms

After the simulation of capacitor cross-coupled differential cascode LNA at 2GHz frequency we obtained various results which are shown in the below figures. First to set the power consumption requirement, we have to adjust the DC bias

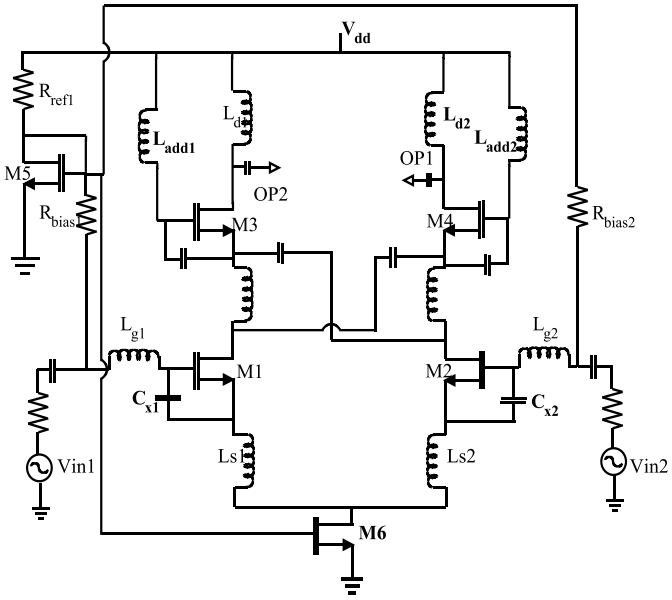

Fig. 4. Capacitor cross-coupled Differential cascade LNA design

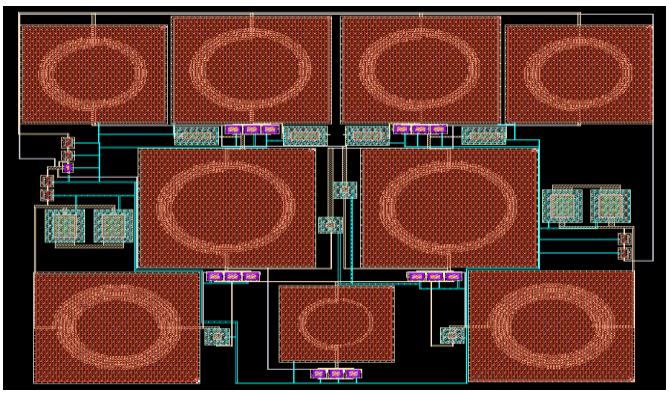

Fig. 6. Layout of capacitor cross-coupled Differential cascade LNA

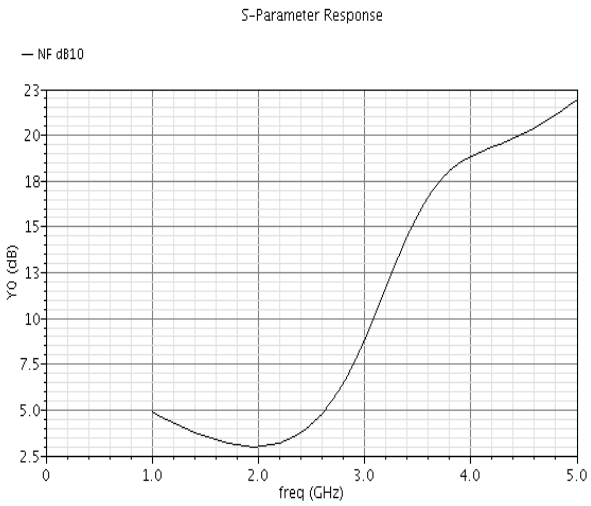

Fig. 7. Plot of noise figure (NF_{min}) at 1.8 V

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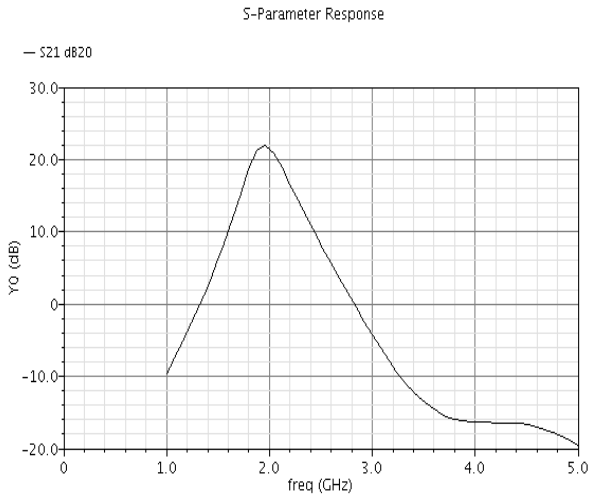

Fig. 8. Plot of power gain at 1.8 V

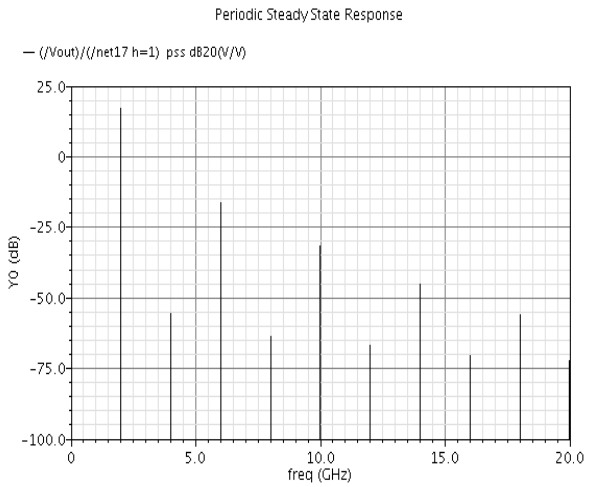

Fig. 9. Plot of voltage gain at 1.8 V

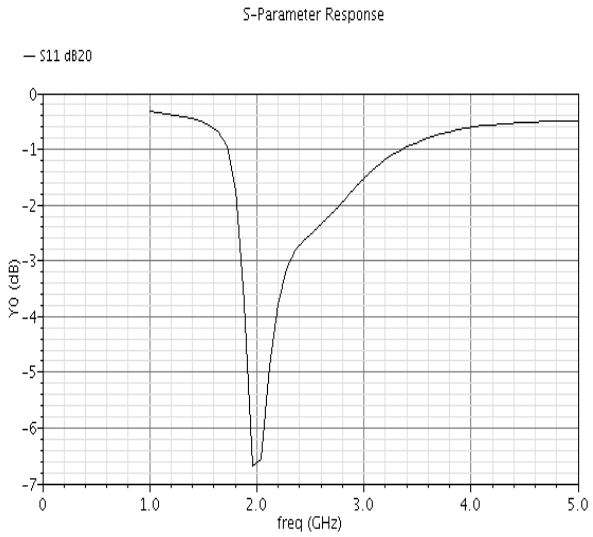

Fig. 10. Plot of S_{11} at 1.8 V

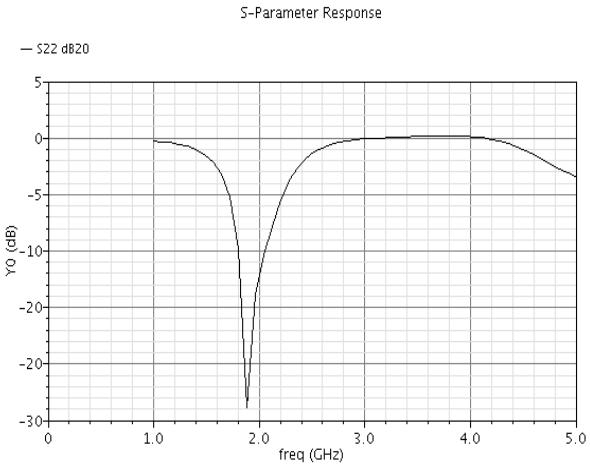

Fig. 11. Plot of S_{11} at 1.8 V

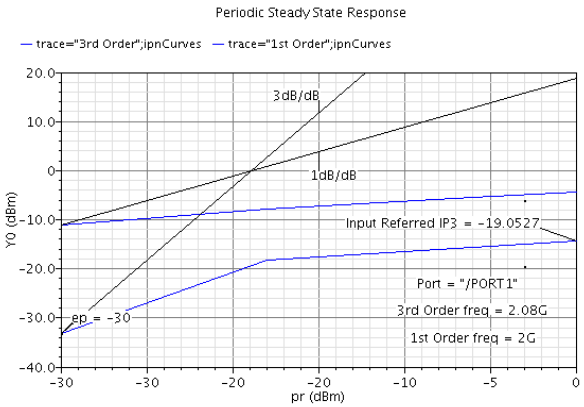

Fig. 12. Plot of IIP3 at 1.8 V

IV. CONCLUSION

In this paper, a capacitor cross-coupled differential cascode LNA has been presented. The simulations of the circuit are carried out using UMC 0.18 µm CMOS process. The differential LNA design, we obtained a noise figure, power consumption, voltage gain and power gain at different supply voltages 1.5 V and 1.8 V are reported here. In this design the gain depends on source inductance and Inter-stage inductor between input stage and cascoded stage boost gain and lower noise figure. The performance results of simulations are compared to some other standard circuits reported. The proposed circuit is observed to consume low power in comparison to the existing circuits.

REFERENCES

i. Somesh kumar and Dr. Ravi Kumar, "A 1.8V and 2GHz Inductively Degenerated CMOS Low Noise Amplifier," International Journal of Electronics Communication and Computer Engineering, Vol. 2, Issue 4, pp. 150-154, july 2012.

ii. Xuan Chen, Quanyuan Feng and Shiyu Li, "Design of a 2.5GHz Differential CMOS LNA," Progress In Electromagnetics Research Symposium, Cambridge, USA, pp. 203-206, Jul. 2008.

iii. *Xuechu LI, Qingyun Gao and Shicai Qin, "An Improved CMOS RF Low Noise Amplifier," Proc. Intl. Conf. ASIC, vol. 2, pp. 1102 - 1105, oct. 2003.*

iv. *Ju Jing and Chunhua Wang, "A New current-mode differential Low Noise Amplifier," ICSICT 2008, 9th International conference, pp. 1524-1527, oct. 2008.*

v. *Thomas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuit," Cambridge University Press, 1998.*

vi. *Shaikh K. Alam and Joanne DeGroat. "A 1.5-V 2.4 GHz Differential CMOS Low Noise Amplifier for Bluetooth and Wireless LAN Applications," CircuitsAnd System, IEEE North-East Workshop on. P13-16 (2006).*

vii. *Somesh kumar and Kuldeepak, "A 0.18µm and 2GHz CMOS Differential Low Noise Amplifier," IJECCT, Vol. 2, Issue 4, pp. 155-158, july 2012.*

viii. *Xiaohua Fan, Heng zhang. "A noise reduction and linearity improvement technique for a differential cascade LNA," IEEE Journal of Solid-state Circuits, 43(3):588-599(2008).*

Parameters	Work done				[4]	[6]	[7]	[8]
	Schematic Results		Post layout results					
Noise Figure (NF_{min}) (dB)	2.049	2.214	6.138	7.285	1.47	2.0	2.4	1.87
Voltage gain (dB)	16.957	11.5406	-2.485	-6.093	N.A	N.A	18.67	N.A
Power gain (dB)	21.42	21.48	1.972	-1.604	12.63	18.9	15.87	10
S_{11} (dB)	-6.612	-5.154	-38.97	-38.57	-26.47	-10.62	-9.842	-13
Power consumption (mW)	6.055	3.887	4.145	2.659	6.49	6.45	16.2	16.2
IIP3 Point (dBm)	-19.05	-21.3546	-14.475	-14.1339	N.A	-13.2	-2.86	-2.05
Frequency (GHz)	2	2	2	2	2.4	2.47	2	2.2
CMOS Process (µm)	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.35
Supply voltage (V)	1.8	1.5	1.8	1.5	1.2	1.5	1.8	1.8

Table I. PERFORMANCE COMPARISION

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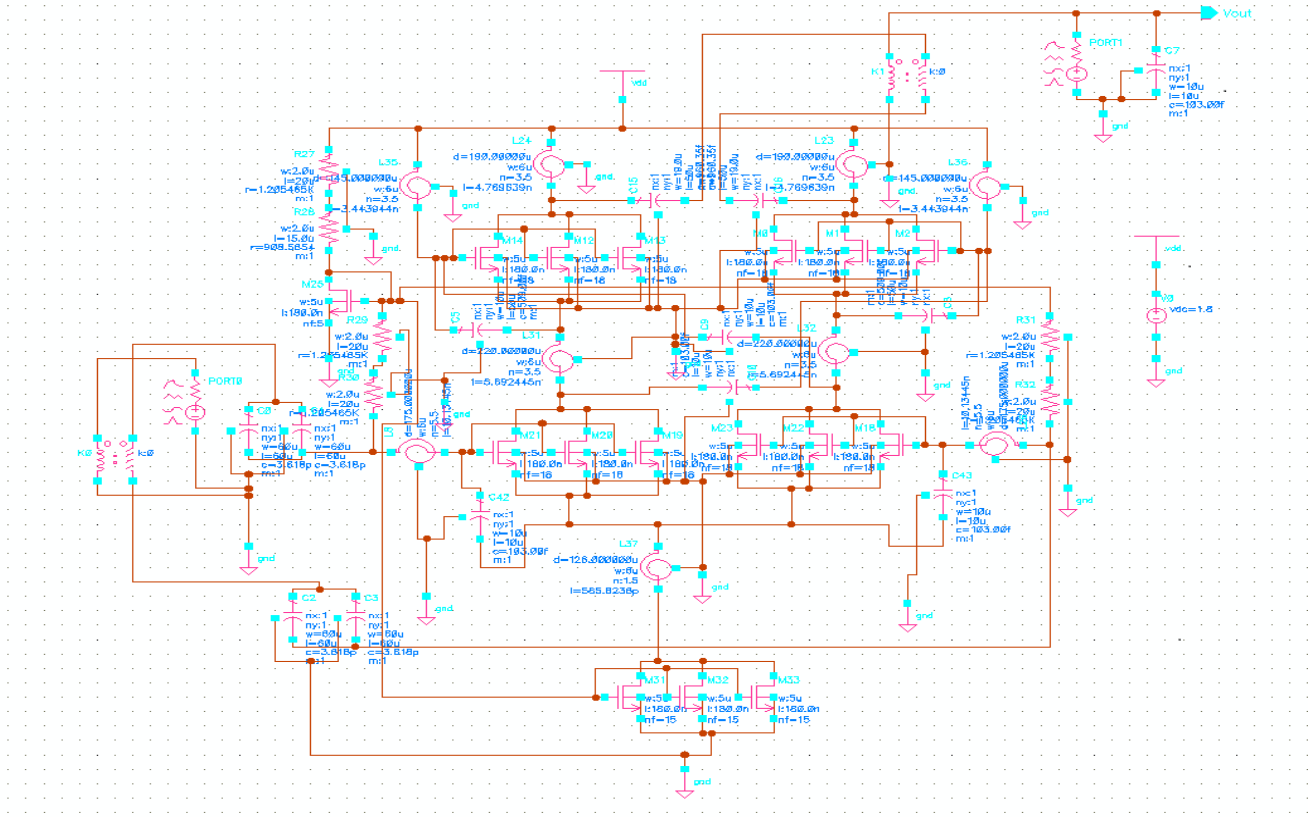

Fig. 5. Schematic of capacitor cross-coupled Differential cascade LNA at 1.8 V