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Low Power Highly Optimized Full Adder By Using Different Techniques With 10 Transistors

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Abstract: The Full Adder circuit is an important circuit in application such as Digital Signal Processing (DSP) architecture, microprocessor, and microcontroller and data processing units. This paper discusses the evolution of full adder circuits in terms of lesser power consumption, higher speed. Starting with the most conventional 28 transistor full adder and then gradually studied full adders consisting of as less as 10 transistors.We included some of the most popular full adder cells like Static Energy Recovery Full Adder (SERF), Adder9B, GDI based full adder. In this paper we simulated the 10T Adder using many techniques. The simulation has been carried out on a Microwind environment tool .

Keywords : CMOS Transmission Gate (TG), Gate Diffusion Input (GDI), Static Energy Recovery Full Adder (SERF), Adder9B.

I. Introduction:

The core of every microprocessor, digital signal processor (DSP), and data processing application like specific integrated circuit (ASIC) is its data path. At the heart of data-path and addressing units in turn are arithmetic units, such as comparators, adders, and multipliers. Finally, the basic operation found in most arithmetic components is the binary addition. Computations need to be performed using low- power, area-efficient circuits operating at greater speed. Addition is the most basic arithmetic operation; and adder is the most fundamental arithmetic component of the processor. The design criterion of a full adder cell is usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU). The limited power supply capability of present battery technology has made power consumption an important figure in portable devices. There is no ideal full adder cell that can be used in all types of applications. Hence novel architectures such as Static Energy Recovery Full Adder (SERF), CMOS Transmission Gate (TG), Adder9B, and GDI based full adder Gate Diffusion Input (GDI) are proposed to meet the requirements. Each design style has its own share of advantages and disadvantages.

The one-bit full adder has a three-input two-output building block. The inputs are the two bits to be summed, A and, B and the carry bit Cj, which derives from the calculations of the last stages digit. The outputs are the result of the sum operation S and the resulting value of the carry bit Co. More expressly the sum and carry output are given by,

Sum = C ex-or (A ex-or B) …… (1)

Carry = (A and B) or C(A ex-or B) …… (2)

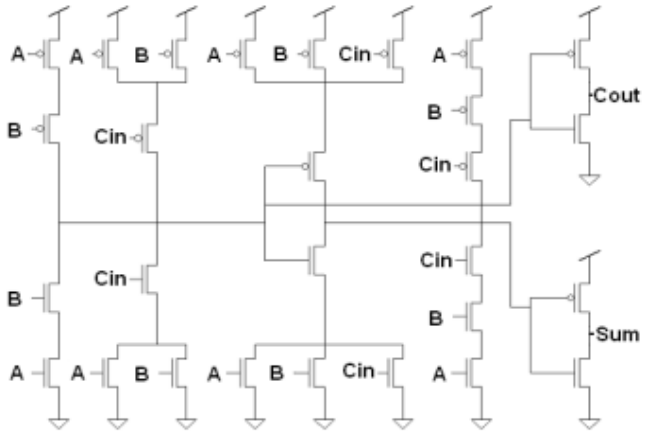
From (2) it is evident that if A=B the carry output is equal to their value. If A* B we have Co = Cj (the full adder is said to be in propagate mode), and hence, the full adder has to stay for the computation of Co.

II . Different Types of Full Adder Circuits:

In this section the different types of full adder circuits are discussed.

A. Conventional 28T CMOS Full Adder Circuit

The conventional CMOS adder cell using 28 transistors based on standard CMOS topology is shown in below figure. Due to high number of transistors, its power consumption is high. Large PMOS transistor in pull up network result in high input capacitances, which cause high delay and dynamic power. One of the most significant advantages of this full adder was ts high noise margins and thus reliable operation at low voltages.

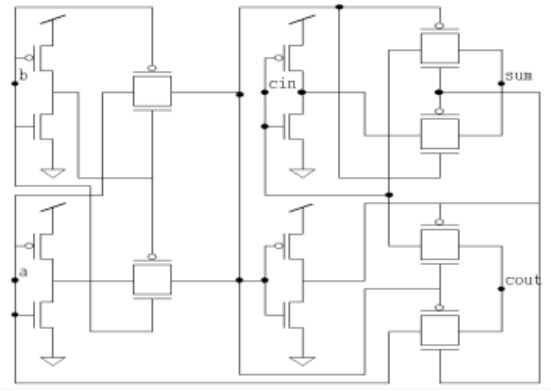


28T Conventional CMOS Full Adder

B. Transmission Gate Full Adder Circuit :

20 T transmission produces buffered outputs of proper polarity for both sum and carry. In this circuit 2 inverters are followed by two transmission gates which act as 8-T XOR. Subsequently 8-T XNOR module follows. To has 4 transistor XOR which in the next stage is inverted to produce XNOR. These XOR and XNOR are used generate sum; **cin** and Cin are multiplexed which can simultaneously to generate sum and cout. The signals cin controlled either by (**a b**) or (**a** ⊗ **b**).Similarly

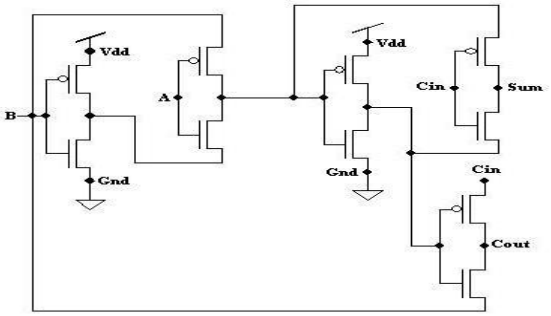
the cout can be calculated by multiplexing **a** and **cin** which is controlled by (**a)**and Cin are multiplexed which can controlled either by (a b) **b**). The power dissipation in this circuit is more than the 28T or (a ⊗ b). Similarly the cout can be calculated by multiplexing a and cin controlled by (a b). The power dissipation in this circuit is more than the 28T adder. However with same power consumption it performs faster .



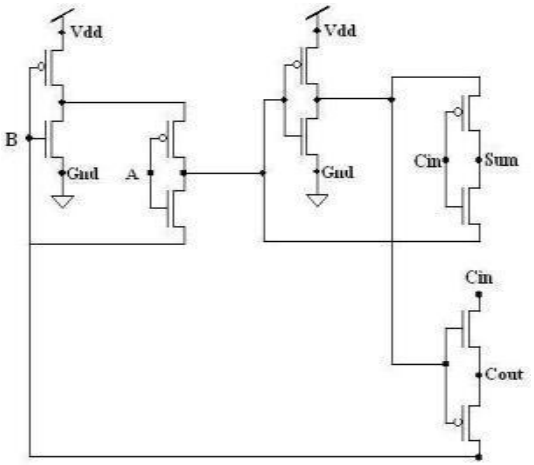
Transmission Gate Full Adder

C. GDI Structure Based Full Adder Circuit :

A new low power design technique that solves most of the problems known as Gate-Diffusion-Input (GDI) is proposed. This technique allows reducing power consumption, propagation delay, and area of digital circuits. A basic GDI cell contains four terminals – G (common gate input of nMOS and pMOS transistors), P (the outer diffusion node of pMOS transistor), N (the outer diffusion node of nMOS transistor), and D (common diffusion node of both transistors).GDI method is based on the use of a simple cell as shown in below figure. At the first look the design is seems to be like an inverter, but the main differences are 1) GDI consist of three inputs- G (gate input to NMOS/PMOS), P (input to source of PMOS) and N (input to source of NMOS). (2) Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter.This design can implement a wide variety of logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors ,while improving logic level swing and static power characteristics and allowing simple top-down design by using small cell library.



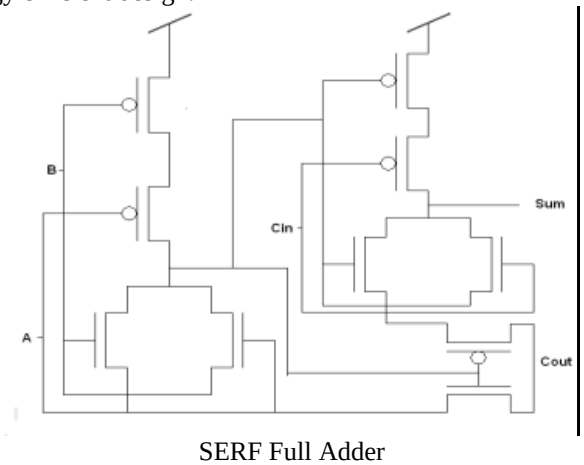
GDI_XOR#ADDER



GDI_XNOR#ADDER

D. Static Energy Recovery Full Adder Circuit :

In the 10T adder cell, the implementation of XOR and XNOR of A and B is done using pass transistor logic and an inverter is to complement the input signal A. This implementation results in faster XOR and XNOR outputs and also ensures that there is a balance of delays at the output of these gates. This leads to less spurious SUM and Carry signal . The energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic. It should be noted that the new SERF adder has no direct path to the ground. The elimination of a path to the ground reduces power consumption. The charge stored at the load capacitance is reapplied to the control gates. The combination of not having a direct path to ground and the re- application of the load charge to the control gate makes the energy-recovering full adder an energy efficient design.



SERF Full Adder

E. ADDER 9B :

The Static Energy Recovery XNOR gate is cascaded with the new G-XNOR gate to generate the Sum while the Cout function is implemented by simply multiplexing B and Cin controlled by (A XNOR B) as done in the previous circuits. These two new adders consistently consume less power in high

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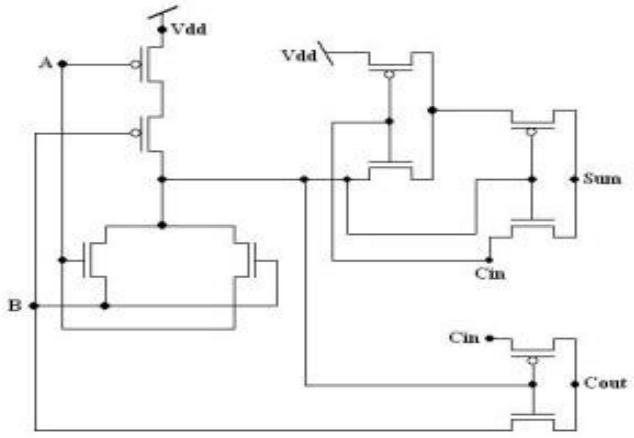
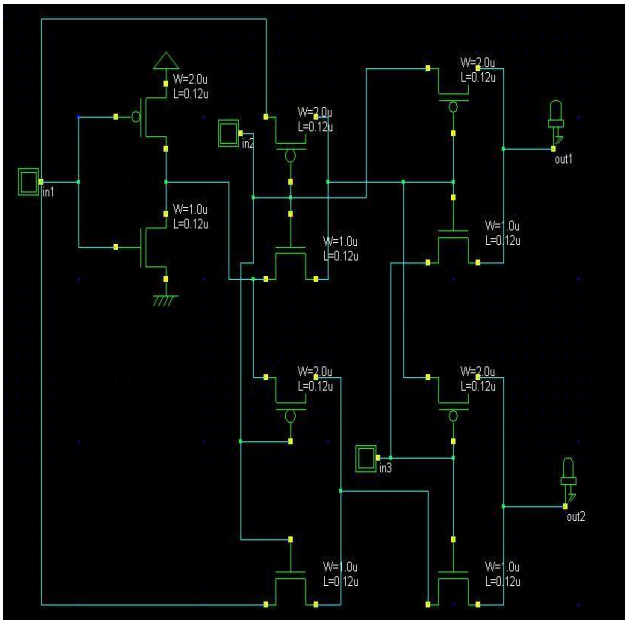
frequencies and have higher speed adder. However with same power consumption it performs faster .



Adder 9B

F. THE PROPOSED l0T FULL ADDER :

The circuit of l0T Adder is a one-bit full adder core has three inputs (A, B, and carry in Ci) and two outputs (sum S and carry out Co). The Adder cell is made of five CMOS inverters that are connected as shown in below figure. Input A is directly connected to inverter first while input B is connected second and third inverter. Second inverter PMOS drain and third inverter NMOS drain are connected first inverter output while second inverter NMOS drain and third inverter drain are connected directly input A. Second inverter output is connected fourth inverter input and input Ci is given in inverter fifth. There is interesting, the power supply V DD connected first inverter only. All transistors have minimum length (LMIN = 45 nm according to used Technology), while their widths are typically propose parameters. The value of WP1 and WP2 defmes PMOS transistors width and WN1 and WN2 defines the NMOS driver transistors width use in first inverter CMOS Inverters.



PROPOSED 10 TRANSISTOR ADDER CELL

III. Simulation Result :

The most conventional 28 transistor full adder and the other conventional full adder cells Static Energy Recovery Full Adder (SERF), Adder9B, GDI based full adder are all simulated using microwind tool.

Table I
Comparative analysis of various type of Full Adder

ADDER	AREA	POWER
CONVENTIONAL FULL ADDER (28T)	62 µm X 12 µm	16.969 µw
TRANSMISSION GATE FULL ADDER (20T)	44 µm X 9 µm	13.495 µw
PROPOSED 10 T FULL ADDER	23 µm X 12 µm	3.670 µw

Table II
Power analysis of various types of 10 T Full Adder

ADDER	POWER
GDI BY XOR	8.906 µw
GDI BY XNOR	7.961 µw
SERA	5.641 µw
10 T PROPOSED	3.670 µw

IV. RESULT :

We use microwind tool for simulation on in different-different technique and circuit parameter in lOT Adder cell and result that the lOT Adder is the most prominent low power consumption cell.

V. References

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