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TCAM Design using parallel pai-sigma matchlines

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ABSTRACT: This work presents a Parallel Pai-Sigma matchline to reduce the compare (search) power of a ternary content addressable memory (TCAM). The pai-sigma matchline does not incur the issues of charge sharing and short circuit current, which typically exist in the hybrid NAND-NOR matchline. The switching activity of the search lines of a TCAM with the pai-sigma matchlines is low. We have implemented the low-power TCAM using CMOS 180 nm, 120 and 65 nm technologies in microwind3.1cadtool. The parallel pai-sigma matchline,When the technology scale down from 180nm to 65nm, power is 1.507µw, delay decreased from 8.566ns to 0.236ns and power-delay product varies from 12.908 to 0.355 x10^{-15} W-s. Ternary content addressable memory (TCAM) is an important component for many applications. For TCAM-based networking systems, the rapidly growing size of routing tables brings with it the challenge to design higher search speeds and lower power consumption.

Index Terms:
Content addressable memories (CAM), low power, networking, ternary CAM (TCAM), Delay

1.INTRODUCTION

Ternary content addressable memories (TCAMs) are widely used in the network applications, such as flow analysis and classless inter-domain routing. In comparison with the random access memory (RAM), however, high power dissipation is one of major disadvantages of the TCAM. Effective power-reduction techniques thus are very important for designing a TCAM.

Some low-power techniques use the concept of matchline partitioning to reduce the power consumption of matchlines. An NOR-type TCAM cell and NAND-tyepe TCAM cell the design of its circuits is presented in section 3 and 4. A ripple-precharge matchline scheme which is similar to an NAND-NOR matchline scheme was proposed to reduce the power dissipation of a TCAM in section 6. For the general applications, the proposed TCAM with parallel Pai-Sigma matchlines has the lowest energy per bit per search in section 7. Transistor-level simulation results are presented in section 8. Finally the conclusion drawn from this work is discussed in section 9.

2. TCAM STRUCTURE

Content-Addresable memory (CAM) compares input search data against a table of stored data, and returns the address of the matching data. CAMs have a single clock cycle throughput making them faster than other hardware- and software-based search systems. CAMs can be used in a wide variety of applications requiring high search speeds.

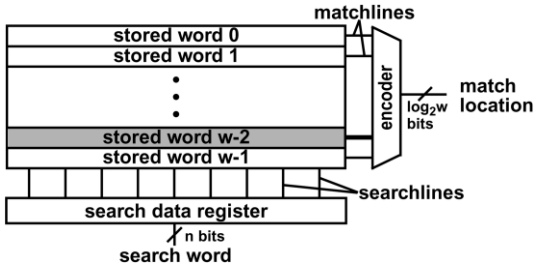

Fig1.TCAM block diagram

Fig.1 shows a simplified block diagram of a CAM The input to the system is the *search word* that is broadcast onto the searchlines to the table of stored data. The number of bits in a CAM word is usually large, with existing implementations ranging from 36 to 144 bits. A typical CAM employs a table size ranging between a few hundred entries to 32K entries, corresponding to an address space ranging from 7 bits to 15 bits. Each stored word has a matchline that indicates whether the search word and stored word are identical (the match case) or are different (a mismatch case, or miss). The matchlines are fed to an encoder that generates a binary match location corresponding to the matchline that is in the match state. An encoder is used in systems where only a single match is expected. In CAM applications where more than one word may match, a priority encoder is used instead of a simple encoder. A priority encoder selects the highest priority matching location to map to the match result, with words in lower address locations receiving higher priority. In addition, there is often a *hit* signal (not shown in the figure) that flags the case in which there is no matching location in the CAM. The overall function of a CAM is to take a search word and return the matching memory location. One can think of this operation as a fully programmable arbitrary mapping of the large space of the input search word to the smaller space of the output match location.

2.1. Ternary Cells:

The NOR and NAND cells that have been presented are binary CAM cells. Such cells store either a logic "0" or a logic "1". Ternary cells, in addition, store an "X" value. The "X" value is a *don't care*, that represents both "0" and "1", allowing a wildcard 1operation.Wildcard operation means that an "X" value stored in a cell causes a match regardless of the input bit.

3. NOR TCAM Cell

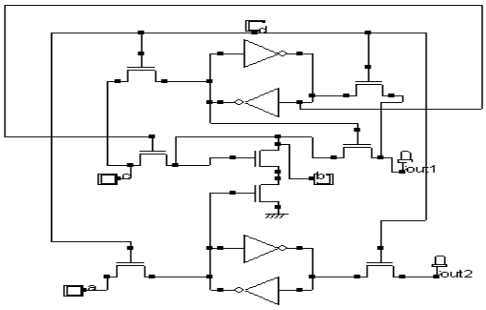

Figure 2: NOR TCAM Cell

The NOR cell implements the comparison between the complementary stored bit D (D bar), and the complementary search data on the complementary searchline, SL(and SLbar), using four comparison transistors, which are all typically minimum-size to maintain high cell density. These transistors implement the pulldown path of a dynamic XNOR logic gate with inputs SL and D. Each pair of transistors, m1/m3 and m2/m4, forms a pulldown path from the matchline, ML, such that a mismatch of SL and D activates least one of the pulldown paths, connecting ML to ground. A match of SL and D disables both pulldown paths, disconnecting ML from ground. The NOR nature of this cell becomes clear when multiple cells are connected in parallel to form a CAM word by shorting the ML of each cell to the ML of adjacent cells. The pulldown paths connect in parallel resembling the pulldown path of a CMOS NOR logic gate. There is a match condition on a given ML only if every individual cell in the word has a match.

4. NAND-Type TCAM cell

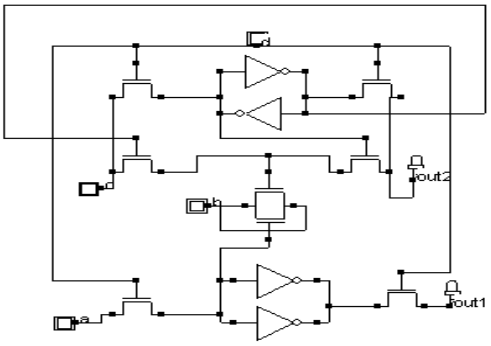

Figure 3: NAND-Type TCAM Cell

The NAND cell implements the comparison between the stored bit, D, and corresponding search data on the corresponding searchlines,(SL,SLbar), using the three comparison transistors,m1,md, and md bar, which are all typically minimum-ize to maintain high cell density. We illustrate the bit-comparison operation of a NAND cell through an example. Consider the case of a match when SL=1 and D=1. Pass transistor M_D is ON and passes the logic "1" on the SL to node B. Node B is the bit-match node which is logic "1" if there is a match in the cell. The logic "1" on node B turns ON transistor M1. Note that M1 is also turned ON in the other match case when SL=0 and D=0. In this case, the transistor $M_{D\ bar}$ passes a logic high to raise node B. The remaining cases, where SL not equal to D,result in a miss condition, and accordingly node B is logic "0" and the transistor is OFF. Node B is a pass-transistor implementation of the XNOR function. The NAND nature of this cell becomes clear when multiple NAND cells are serially connected. In this case the ML_n and ML_{n+1} nodes are joined to form a word. A serial nMOS chain of all the transistors resembles the pulldown path of a CMOS NAND logic gate. A match condition for the entire word occurs only if every cell in a word is in the match condition.

5. Single Pai-Sigma Matchline Structure:

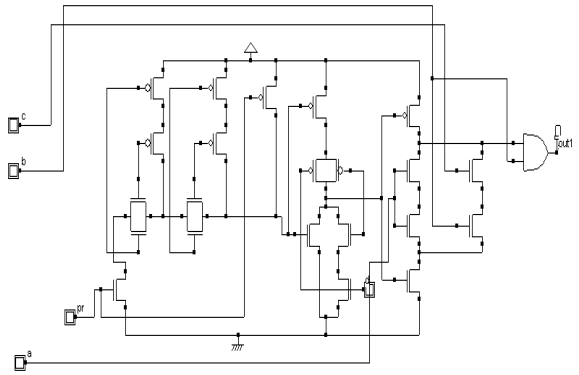

Figure 4: Single Pai-Sigma Matchline

Fig.4 shows the transistor-level diagram of the proposed Pai-Sigma matchline scheme, where only the comparison logic of the TCAM cells is shown. The Pai segment realizes NAND function, $\pi_{i=0}^{p-2}(S_i+M_i)$.The Sigma segment realizes NOR function, $\sum_{j=p}^{n-1}(S_{bar.j}.M_{bar.j})$. The $cell_{p-1}$ is merged with the interface logic between the Pai segment and Sigma segment. For the Pai segment, i.e., $Cell_0$ to $Cell_{p-2}$, the comparison logic of each cell is comprised of two nMOS transistors in shunt and two pMOS transistors in series. Each pair of pMOS and nMOS transistors is controlled by S_i and M_i. For the Sigma segment, i.e. $Cell_p$ to $Cell_{B-1}$, the comparison logic of each cell is two nMOS transistors in series. The comparison logic of the $Cell_{p-1}$ is mixed with the interface logic. Hybrid NAND-NOR matchline is one favorite design approach to achieve the compromise between the power and delay of a matchline. When the CAM performs a Compare operation, all the NAND

matchlines are activated. But, only the NOR matchlines with the corresponding NAND matchlines generating a match result are activated. Since the switching power of the NAND matchline is low and only a small amount of NOR matchlines are activated,the compare power of the CAM with NAND-NOR matchlines can drastically be reduced. Also, the delay of the NAND-NOR matchline is better than that of the NAND matchline.

6. Ripple-Precharge TCAM:

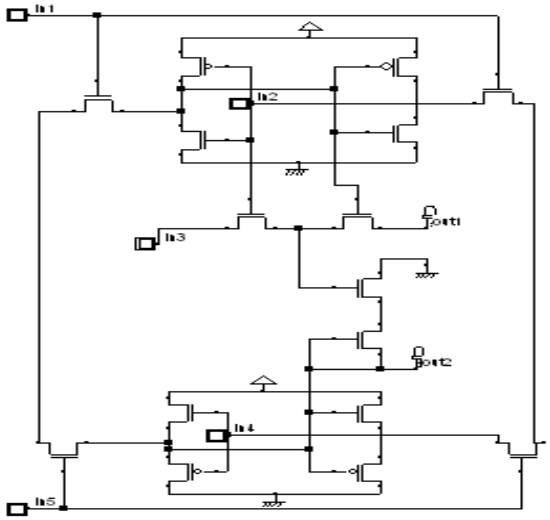

Figure 5: Ripple-Precharge TCAM

Figure 5 shows the basic structure of the conventional TCAM bit. The TCAM model we have assumed consists of three main components - a 8T CAM cell which stores the data bit and also compares its content (D) with the key (CMP), a 6T SRAM cell which stores the mask bit (MD) and a 2T XOR gate that compares the result of the CAM operation (X) with complement of mask bit (MDB) to determine whether we have a match or not. The contents of both the SRAMs are read and written using the bit lines (BL) and (BLB). (WL) and (MWL) lines are made active high for any Read/Write operation involving data or mask bit. The comparand or key for the search operation is fed to the CAM cell using the comparand lines (CMP and CMPB). The match line (ML) which is connected to one end of the 2-input XOR gate is precharged to Vdd before any search operation while other end is connected to ground. The 2-input XOR gate is controlled by the output of the CAM cell (X) and the mask bit (MDB). Depending on the output of CAM cell and the mask bit, the ML either discharges when there is a mismatch or retains the charge on match. Typically during a mismatch, the mask bit MD=1 shows that the bit is a "care" bit and the CAM cell output X =1 shows that there is a mismatch between data and key.

7. Parallel Pai-Sigma Matchline Structure (P^2SML):

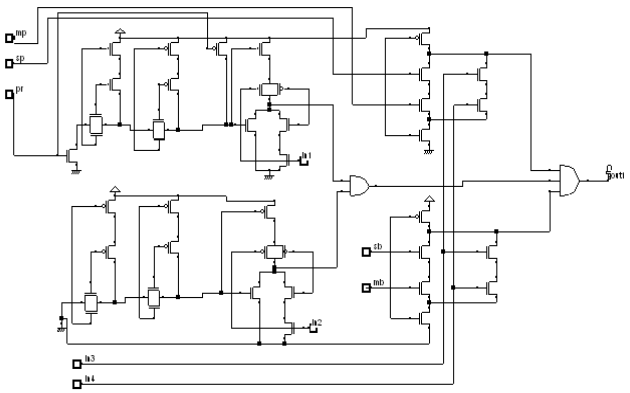

Figure 6: P^2S Matchline Structure

Fig. 6 shows the proposed P^2SML scheme, where the Pai segment is separated into the PaiA and PaiB; and the Sigma segment is separated into the SigmaC and SigmaD. The precharge operation of the SigmaC and SigmaD is controlled by the result of ML_{pai}. If the comparison result of the Pai segment is match, the ML_{pai} =0 and the matchlines of SigmaC and SigmaD are precharged to V_{dd}. The ML_{pai} is the AND of ML_{PaiA} and ML_{PaiB}. Thus, if either ML_{PaiA} or ML_{PaiB} is at logic 0 (in precharge phase or a miss result), then the ML_{Pai} is 0 and the matchlines of SigmaC and SigmaD can be precharged to V_{dd}. Therefore, only a precharge control circuit is implemented in the PaiA segment, which can guarantee the ML to be set to logic 0 in the precharge phase. This can also reduce the power consumption contributed by the precharge signal.

8. IMPLEMENTATION RESULTS

Table1: NOR TCAM Cell

Technology (nm)	Power(µW)	Delay(ns)	Area(Pm)	PDP(10^{-15}W-s)
CMOS 180	1.305	1.412	51.21	8.782
CMOS 120	1.305	0.992	51.92	1.294
CMOS 65	1.305	0.040	52.25	0.248

Table2: NAND TCAM Cell

Technology (nm)	Power(µW)	Delay(ns)	Area(Pm)	PDP(10^{-15}W-s)
CMOS 180	21.064	2.018	51.405	42.507
CMOS 120	21.064	1.418	51.266	29.868
CMOS 65	21.064	0.058	51.405	1.221

Table3: Single pai- sigma matchline

Technology (nm)	Power(µW)	Delay(ns)	Area(Pm)	PDP(10^{-15}W-s)
CMOS 180	1.470	3.127	119.36	4.596
CMOS 120	1.470	2.197	124.26	3.229
CMOS 65	1.470	0.100	121.20	0.122

Table4: Ripple-Precharge TCAM

Technology (nm)	Power(µW)	Delay(ns)	Area(Pm)	PDP(10^{-15}W-s)
CMOS 180	5.012	4.127	72.575	20.490
CMOS 120	5.012	3.317	72.462	14.383

CMOS 65	5.012	0.121	72.462	0.541

Table5: Parallel Pai- Sigma Matchline

Technology (nm)	Power(µW)	Delay(ns)	Area(Pm)	PDP(10^{-15}W-s)
CMOS 180	1.507	8.566	320.47	12.908
CMOS 120	1.507	6.016	327.99	9.0661
CMOS 65	1.507	0.236	333.43	0.3556

Table 1 Represents the NOR Type TCAM cell for that circuit, in the case of 65nm technologies power is same compare with the previous technologies such as 120nm and 180nm.but the performance is well compare with the previous technologies. Delay and area is also very well compare with the previous technologies and PDP is also observed for this circuit power is 1.305µw, delay is 0.040ns, area is 52.25pm.
Table 5 Represent the parallel pai-sigma matchline, when the technology scale down from 180nm to 65nm, power is 1.507µw, delay decreased from 8.566 to 0.236ns and power-delay product varies from $12.908x10^{-15}$ to $0.355x10^{-15}$W-s.

9. CONCLUSSIONS:

In this work we have presented a low power TCAM using the parallel Pai-Sigma matchline which does not incur the issues of charge sharing and the DC path. The switching activity of the search lines is also low. We have implemented the low-power TCAM using CMOS180nm, 120nm and 65 nm technologies in microwind3.1cadtool. The parallel pai-sigma matchline When the technology scale down from 180nm to 65nm, power is 1.507µw, delay decreased from 8.566 to 0.236ns and power-delay product varies from 12.908 to 0.355 $x10^{-15}$W-s.

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