International Journal of Engineering Research
Volume No.4, Issue No.7, pp : 346-350
ISSN:2319-6890)(online),2347-5013(print)
01 July 2015

# Implementation of Regular Linear Carry Select Adder with Binary to Excess-1 Converter

**K.Bala Sindhuri**
Department of Electronics & Communincation Engineering
Assistant Professor,S.R.K.R Engineering College,Bhimavaram
k.b.sindhuri@gmail.com

***Abstract**: Regular Linear Carry Select Adder (RCSLA) is one of the fastest adders. From the structure of RCSLA, there is scope to reduce area by using Binary to Excess-1 converter (BEC) technique. By using BEC technique in RCSLA 16, 32, 64 bit architectures have been developed and compared with Regular Linear Carry Select Adder. The modified architectures have reduced area and power with slight increase in delay. Simulation and Synthesis are carried on Xilinx ISE 12.2.The result analysis shows that the modified architectures are better than RCSLA.*

**Key words -Binary to Excess one Converter (BEC), Ripple Carry Adder (RCA), Full Adder (FA),Half Adder(HA), FPGA(Field Programmable Gate Array), KSA(Kogge Stone Adder**)

## I. INTRODUCTION

Design of Low area- and low power are the most substantial areas of research in VLSI system design. BINARY addition is one of the primitive operations in computer arithmetic. VLSI integer adders are critical elements in general purpose and digital-signal processing processors since they are employed in the design of Arithmetic-Logic Units, in floating-point arithmetic data paths and in address generation units. They are also employed in encryption and hashing function implementation. In digital adders[1],Carry plays the major role which limits the speed of addition. The sum for each bit position in a basic digital adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position which increases the delay of the addition.

RCSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum . However, the RCSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input and selected by the multiplexers (mux), then the final sum and carry are selected by the multiplexers (mux).The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with lower area and power consumption [2]–[4]. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure. The details of the BEC logic are discussed in Section III.

This brief is structured as follows. Section II deals with the delay and area evaluation methodology of the basic adder blocks. Section III presents the detailed structure and the function of the RCA logic.Section IV presents the detailed structure and the function of the BEC logic. RCSLA has been chosen for comparison with the modified designs as they have requires lower power and area The delay and area evaluation methodology of the regular and modified RCSLA's are presented in Sections 1V, V respectively. The FPGA implementation details and results are analyzed in Section VI. Finally, the work is concluded in Section VII.

## II. DELAY AND AREA EVALUATION METHODOLOGY OF THE BASIC ADDER BLOCKS

The AND, OR, and Inverter (AOI) implementation of an Half Adder is shown in Fig. 1. The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 Multiplexer, XOR,HA, and FA, are evaluated and listed in Table I.

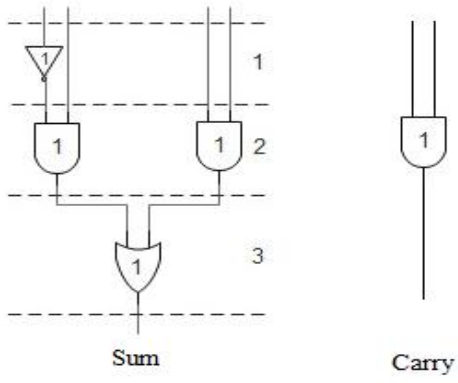


Fig.1.Delay and Area Evaluation of Half Adder.

ISSN:2319-6890)(online),2347-5013(print)
01 July 2015

Table I
Delay and Area count of the Basic adder Blocks

| Adder Blocks | Area | Delay |
|---|---|---|
| Xor | 5 | 3 |
| 2:1 Mux | 4 | 3 |
| HA | 6 | 3 |
| FA | 13 | 6 |

## III.DELAY AND AREA EVALUATION METHODOLOGY OF THE RIPPLE CARRY ADDER FOR 4-BIT

Ripple Carry adder consists of 4 Full adders. Each full adder consists of 2 half adders and an or gate. Delay and area evaluation for each full adder in Ripple Adder is explained as follows.

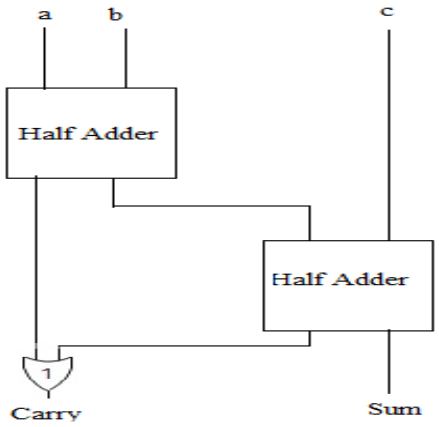


Fig.2.Full Adder using Half Adder

1. Arrival time for sum (0) is 6 units of time where as for carry (0) is 5 units of time.
2. Depending on the arrival time of carry (0), Arrival time for Sum (1) is 8 units of time where as for carry (1) is 7 units of time
3. Depending on the arrival time of carry (1), Arrival time for Sum(2) is 10 units of time where as for carry(2) is 8 units of time.
4. Depending on the arrival time of carry (2), Arrival time for Sum(3) is 12 units of time where as for carry(3) is 11 units of time

Total number of gates is determined as follows
Gate count=52(8 Half adders+ 4 or Gates)
Half adders =48(8*6).
Or Gates=4(4*1).

Table II
Delay and Area count of the Basic adder Blocks

| RCSLA Blocks | Area | Delay |
|---|---|---|
| 4 Bit RCA With Cin=0 | 45 | 10 |
| 4 Bit RCA With Cin=1 | 52 | 12 |

III. Binary to Excess -1 Converter

The basic idea to use Binary to Excess-1 Converter (BEC) in the regular CSLA to achieve lower area. This logic is replaced in Linear CSLA with "Cin=1". This logic can be implemented for different bits which are used in the modified design. The main advantage of this BEC logic comes from the fact that it uses lesser number of logic gates than the n-bit Full Adder (FA) structure As stated above the main idea of this work is to use BEC instead of the KSA with "Cin=1" in order to reduce the area in the regular CSLA to obtain modified CSLA. To replace the n-bit RCA, an (n+1) bit BEC logic is required. The structure of a 5-bit BEC is shown in Fig.3 and the function table of 5-bit BEC is shown in Table.III

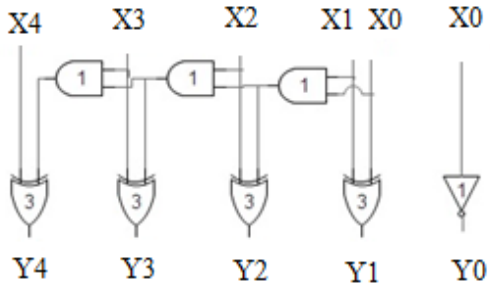


Fig.3.Binary to Excess-1 converter

Table.III.

| X[4:0] | Y[4:0] |
|---|---|
| 00000 | 00001 |
| 00001 | 00010 |
| 00010 | 00010 |
| 11111 | 00000 |

Function Table of the 5 bit BEC.

Delay and area evaluations for 5 bit BEC is explained as follows

1. Arrival time for Y0 is 1 unit of time where as arrival times for Y1,Y2,Y3,Y4 are 3,4,5,6 units of time respectively
2. Total number of gates is determined as follows
   Gate count=24(3 And gates+ 4 Xor Gates+ 1 not gate)
   And gates=3(3*1).
   Not gate =1(1*1).
   Xor Gates=20(4*5).

## IV.Delay and Area evaluation Methodolgy of Regular Linear CSLA

Regular Linear CSLA for n-bit consists of n/4 groups with 1st group of 4bit RCA with Cin and remaining (n/4)- 1 groups consists of 4 bit RCA's with Cin=0 & Cin=1

### IV.1.Linear CSLA for 16 bit:

ISSN:2319-6890)(online),2347-5013(print)
01 July 2015

It consists of 4 groups.The steps leading to area and delay evaluations are given below

1. Group1 consists of 4 bit Ripple Carry adder. It consists of4 Full adders. Arrival time for sum(0) is 6 units, where as arrival times for sum(1),sum(2),sum(3) are 8,10,12 units of time respectively. Similarly ,Arrival time for Carry(0) is 5 units, where as arrival times for Carry (1), Carry (2), Carry (3) are 7,9,11 units of time respectively
2. Group2, Group3, Group4 each consists of 2 sets of 4 bit Ripple Carry adders and multiplexers. Each Group consists of 7 Full adders, 1 Half adder and 5 multiplexers. Arrival times for s (4),s (5),s (6),s (7),c(7) of 2nd set of RCA for input carry value equal to 1 are 6,8,10,12,11 units of time respectively. Depending on Carry(3) from Group1,which is applied as selection input for multiplexer, Arrival time for Sum(4), Sum(5), Sum(6), Sum(7) are 14,14,14,15 where as arrival time for Carry (7) is 14 units of time respectively
3. Arrival times for s (8),s (9),s (10),s (11) ,c(11)of 2nd set of RCA for input carry value equal to 1 are 6,8,10,12,11 units of time respectively. Depending on Carry(7) from Group2,which is applied as selection input for multiplexer, Arrival time for Sum(8), Sum(9), Sum(10), Sum(11) ,Carry(11) are 17 units of time respectively
4. Arrival times for s (12),s (13),s (14),s (15) ,c(15)of 2nd set of RCA for input carry value equal to 1 are 6,8,10,12,11units of time respectively. Depending on Carry(11) from Group2,which is applied as selection input for multiplexer, Arrival time for Sum(12), Sum(13), Sum(14), Sum(15), Carry(15) are 20 units of time respectively.

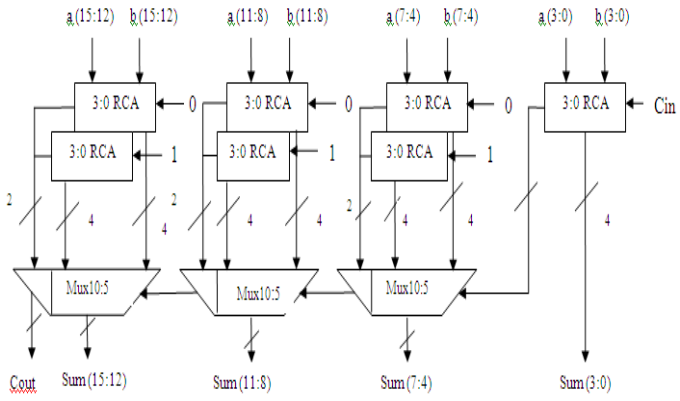


Fig.4.Regular Linear Carry Select Adder

Based on the Area count listed in Table I,the total no.of gates in Group2 ,Group3,Gropup4 is determined as follows

Gate count=117(FA+HA+MUX)
FA=91(7*13).
HA=6(1*6).
MUX=20(5*4).

Table IV
Delay and Area Evaluation for Linear CSLA

| Group | Area | Delay |
|---|---|---|
| Group1 | 104 | 12 |
| Group2 | 117 | 15 |
| Group3 | 117 | 17 |
| Group4 | 117 | 20 |

The total area count for Linear Kogge stone CarrySelect Adder[5] for 16 bit is 515 gate areas where as for Regular Linear CSLA is 455 gate areas. Even though Maximun Delay is same, Area is further reduced.

IV.II. Regular Linear CSLA for 32 bit: It consists of 8 groups. The Steps leading to delay & Area Evaluation Methodology are given below

Group1 to Group 4 Area and delay methodology is same as 16 bit RCSLA.

1. The max delay for Group5,Group6, Group7, Group8 is 23,26,29,32 depending on the arrival of c(15),c(19),c(23),c(27).

   Total Area count for Regular Linear CSLA is 923 gates.

I. Regular Linear CSLA for 64 bit: It consists of 16 groups. The Steps leading to delay & Area Evaluation Methodology are given below

Group1 to Group 8 Area and delay methodology is same as 32 bit RCSLA.

1. The max delay for Group9,Group10, Group11, Group12, Group13, Group14, Group15,Group16is 35 ,38 ,41 ,44, 47 , 50 ,53 ,56 depending on the arrival of c(31),c(35),c(39),c(43),c(47),c(51),c(55), c(59).

2. Total Area count for Regular Linear CSLA is 1859 gates

V.DELAY AND AREA EVALUATION METHODOLGY OF MODIFIED LINEAR CSLA WITH BEC

The structure of 16 bit Modified Linear Carry Select Adder With BEC is shown in Fig5.Instead of 2nd set of RCA with input carry1, BEC for 5 bit is replaced.

V.I. Modifies Linear CSLA for 16 bit:Linear CSLA with BEC for 16 bit also consists of 4 groups. The steps leading to delay andarea evaluations are given below

1. Group1 consists of 4 bit Ripple Carry adder. It consists of 4 full adders. Arrival time for sum(0) is 6 units, where as arrival times for sum(1),sum(2),sum(3)

ISSN:2319-6890)(online),2347-5013(print)
01 July 2015

are 8,10,12 units of time respectively. Similarly ,Arrival time for Carry(0) is 5 units, where as arrival times for Carry (1), Carry (2), Carry (3) are 7,9,11 units of time respectively

2. Group2,Group3,Group4 each consists of 1 set of 4 bit Ripple Carry adder ,1 set of BEC and multiplexers.It consists of 3 full adders ,1 Half adder and 5 multiplexers. Arrival times for s(4),s(5),s (6),s (7),c(7) of 5 bit BEC for which inputs are taken from 4 bit RCA are 7,9,11,13,16,17 units of time respectively. Depending on Carry(3) from Group1,which is applied as selection input for multiplexer, Arrival time for sum(4), Sum(5), Sum(6), Sum(7) are 13,13,13,16 where as arrival time for Carry (7) is 17 units of time respectively
3. Arrival times for s (8),s (9),s (10),s (11),c(11) of 5 bit BEC for which inputs are taken from 4 bit RCA are 7,9,11,13,16,17 units of time respectively. Depending on the Carry(7) from Group2,which is applied as selection input for multiplexer.Arrival time for sum(8),Sum(9),Sum(10),Sum(11),carry(11)are evaluated as 20 units of time respectively
4. Arrival times for s (12),s (13),s (14),s (15),c(15) of 5 bit BEC for which inputs are taken from 4 bit RCA are 7,9,11,13,16,17 units of time respectively. Depending on the Carry (11) from Group3,which is applied as selection input for multiplexer, Arrival time for sum(12), Sum(13), Sum(14), Sum(15), carry(15) are evaluated as 23 units of time respectively.

Based on the Area count listed in Table I,the total no.of gates in Group2,Group3,Group4 is determined as follows

Gate count=117( FA+ HA+ MUX+ NOT+ AND+ XOR)

FA=39(3*13).
HA=6(1*6).
MUX=20(5*4).
XOR=20(4*5).
AND=3(3*1).
NOT=1(1*1).

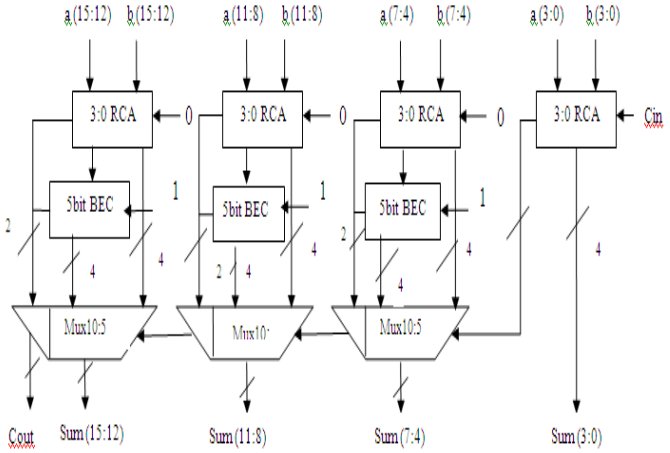


Fig.5.Regular Linear Carry Select Adder with BEC

TableV
Delay and Area Evaluation for Linear CSLA with BEC

| Group | Area | Delay |
|---|---|---|
| Group1 | 104 | 12 |
| Group2 | 89 | 17 |
| Group3 | 89 | 20 |
| Group4 | 89 | 23 |

Comparing TablesIV,V It is clear that Modified Linear CSLA with BEC saves 84 gates with 3 units increase in delay.

V.II.Modified Linear CSLA for 32 bit: It consists of 8 groups. The Steps leading to delay & Area Evaluation Methodology are given below

1. Group1 to Group 4 Area and delay methodology is same as 16 bit RCSLA.
2. The max delay for Group5,Group6, Group7, Group8 is 26,29,32,35 depending on the arrival of c(15),c(19),c(23),c(31).

Total Area count for Modified Regular Linear CSLA is 727 gates.

V.III.Modified Linear CSLA for 64 bit: It consists of 16 groups. The Steps leading to delay & Area Evaluation Methodology are given below

Group1 to Group 8 Area and delay methodology is same as 32 bit RCSLA.

The max delay for Group9,Group10, Group11, Group12, Group13, Group14, Group15,Group16is 38 ,41 ,44, 47 , 50 ,53 ,56,59 depending on the arrival of The max delay for Group5,Group6, Group7, Group8 is 26,29,32,35 depending on the arrival of c(31), c(35), c(39), c(43), c(47),c(51),c(55), c(59).

Total Area count for Modified Linear CSLA is 1083 gates

## VI. Results and Tables

Simulation Results for 16bit, 32 bit, 64 bit.

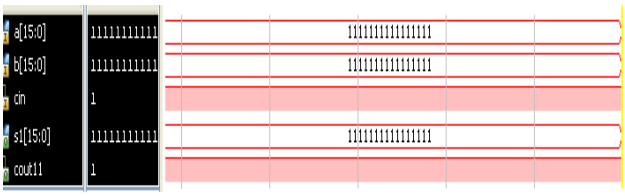


Fig6.Simulation Result for 16 bit RCSLA

ISSN:2319-6890)(online),2347-5013(print)
01 July 2015

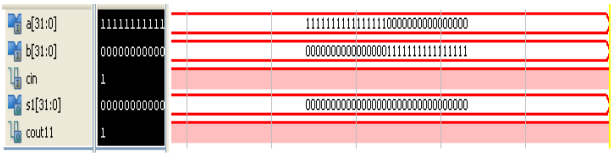


Fig7.Simulation Result for 32 bit RCSLA


Fig8.Simulation Result for 64 bit RCSLA

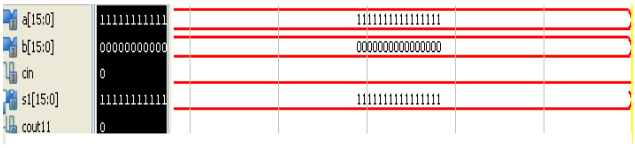


Fig9.Simulation Result for 16 bit RCSLA with BEC


Fig10.Simulation Result for 32 bit RCSLA with BEC

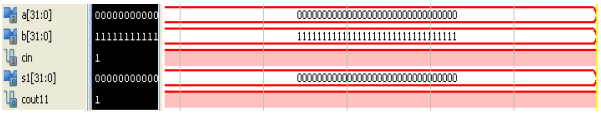


Fig11.Simulation Result for 64 bit RCSLA with BEC
TABLE.V.

Summary results for Linear RCSLA for 16 bit

| Logic Utilization | Used | Available |
|---|---|---|
| Number of Slices | 424 | 4656 |
| Number of 4 input LUTs | 413 | 9312 |
| Number of bonded IOBs | 53 | 232 |

TABLE.VI.
Summary results for Modified RCSLA with BECfor 16 bit.

| Logic Utilization | Used | Available |
|---|---|---|
| Number of Slices | 424 | 4656 |
| Number of 4 input LUTs | 413 | 9312 |
| Number of bonded IOBs | 53 | 232 |

TABLE.VII.

Power and Frequency for RCSLA & Modified RCSLA using BEC for 16 bit

| Parameter | RCSLA | Modified RCSLA with BEC |
|---|---|---|
| Total Power | 83.38mW | 83.48 mW |
| Dynamic Power | 2.37 mW | 2.47 mW |
| Quiescent Power | 81.01 mW | 81.01 mW |
| Frequency | 70.185 MHZ | 68.512 MHZ |

VII.CONCLUSION

A simple approach is presented in this paper to improve the performance of Linear RCSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area.

## References

i. *O. J. Bedrij, "Carry-select adder," IRE Trans. Electron. Comput., pp.340–344, 1962.*

ii. *B. Ramkumar, H.M. Kittur, and P. M. Kannan, "ASIC implementationof modified faster carry save adder," Eur. J. Sci. Res., vol. 42, no. 1, pp.53–58, 2010.*

iii. *T. Y. Ceiang and M. J. Hsiao, "Carry-select adder using single ripplecarry adder," Electron. Lett., vol. 34, no. 22, pp. 2101–2103, Oct. 1998.*

iv. *Y. Kim and L.-S. Kim, "64-bit carry-select adder with reduced area,"Electron. Lett., vol. 37, no. 10, pp. 614–615, May 2001.*

v. *B.Tapasvi,K.BalaSindhuri,I.Chaitanya Varma,Prof.N.UdayaKumar " Implementation of 64 Bit KoggeStone Carry Select Adder with BEC For Efficient Area" IJRECE VOL. 3 ISSUE 1 JAN-MAR 2015 ISSN: 2393-9028 (PRINT) | ISSN: 2348-2281 (ONLINE)*