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Design of Low power, Dead zone free CMOS PFD for PLL

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***Abstract*—This paper presents an improved design of phase frequency detector for Phase Locked Loop (PLL), which retains the main characteristics of PFD. The proposed design uses 18 transistors operated at 1.8V power supply and it consumes power of 42.7uW when reference input frequency clock operates at 400MHz. The dead zone has been completely eliminated. The design is implemented in cadence virtuoso using gpdk180nm CMOS process technology.**

Keywords— Dead zone, PFD, PLL.

I. INTRODUCTION

The PLL was introduced in early 1930's. PLL has got wide usage in electronics and communication. PLL has been implemented in many technologies, but till today the deigning of PLL is a complex job for the designer. PLL has got wide variety of applications such as frequency synthesizer, microprocessor, radio receiver, frequency demodulator, divider etc.

The block diagram of PLL is shown in the figure below. PLL is a feed back control system that causes the output of voltage controlled oscillator (VCO) signal tracks the phase and frequency of external reference signal.

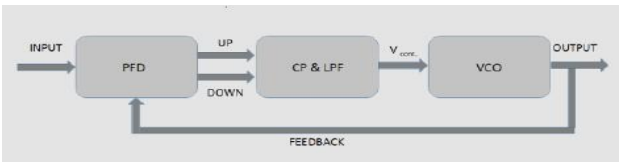


Fig. 1.1 Block diagram of Phase locked loop

A PLL mainly consists of PFD, charge pump, loop filter, voltage controlled oscillator (VCO). In some cases divider circuit is used in feedback path for synthesis operation. The phase frequency detector compares the phase and frequency of reference signal with the feedback signal. Output of PFD is proportional to the phase difference between two input signals.

The discrete error output signal of PFD is converted into continuous time error signal by charge pump and loop filter. The output of the loop filter will be given to voltage controlled oscillator. If the angular frequency of the input signal is equal to the center frequency of the VCO, then PFD will produce zero output consequently loop filter will produce zero output. This condition permits VCO to operate at its center frequency. If this is not the case, then the output of the PDF will be non zero after some time interval the loop filter would produce a finite signal, this would result in change in operating frequency of VCO in such a way that phase error diminishes.

II. LITERATURE REVIEW

Phase detector are classified into two types analog phase detector such as multiplier and another type is digital phase detector such as XOR phase detector, JK phase detector and there are many circuits available that falls under digital phase detector category. The disadvantage is, it can't detect the frequency difference. The characteristics of JK flipflop phase detector is shown if figure 2.1.

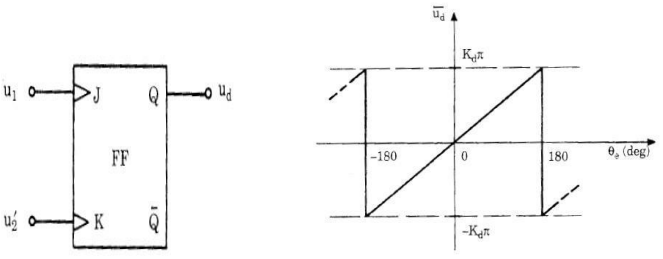
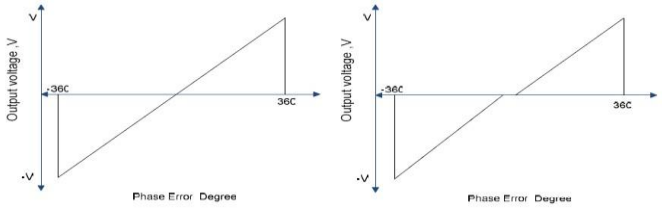


Fig. 2.1 Block diagram of JK flipflop phase detector and its characteristics.

Phase detector can produce correct output only if phase difference lies between -180 deg to +180 deg. The conventional phase frequency detector is shown in figure 2.2. It contains logic gates which are suffering from dead zone, very limited frequency of operation, lock time is slow. Conventional PFD also has inappropriate delay to reset



(a) (b)

Fig 2.3: output voltage vs phase error. (a) No dead zone. (b) Dead zone.

internal nodes which affects the PLL speed. The dynamic phase frequency detectors are used in modern days. Theblock diagram of dynamic phase frequency detector is shown with its state transition diagram in the figure 2.3. This type of detectors enhances accurate operation, high frequency of operation, fast locking, since there is a reset path dead zone is unavoidable.

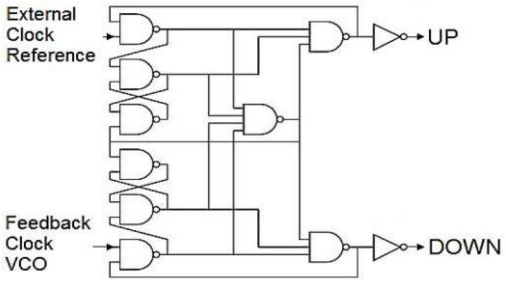


Fig 2.2 Conventional logic gates PFD

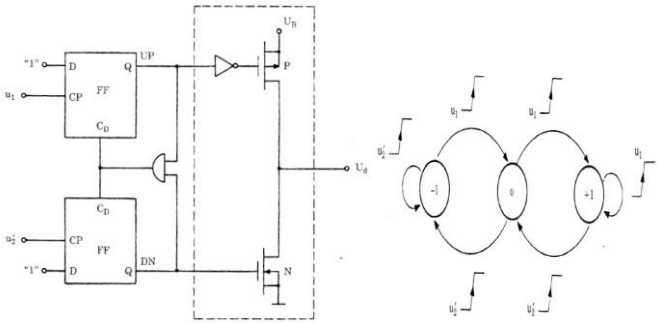
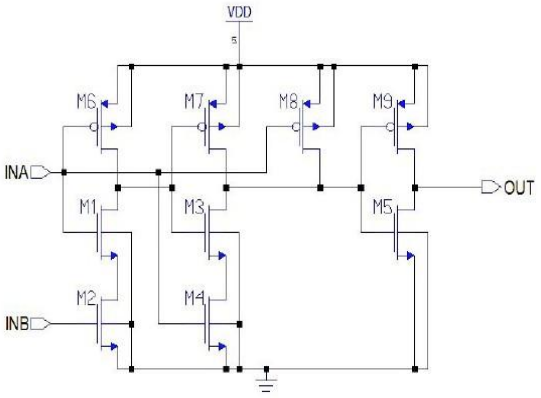
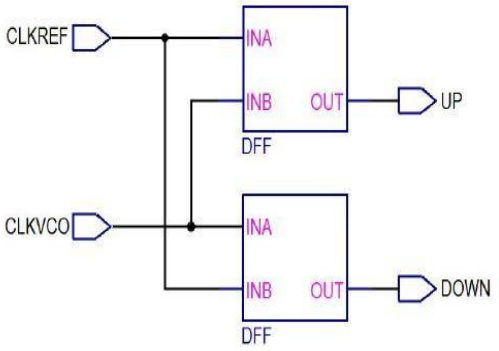


Fig. 2.3.Schematic diagram of the PFD and its state diagram. Phase frequency detector has two inputs that are reference signal and feedback signal and two output signals that are UP and DN as shown in the figure 2.2. The PFD compares the two signals then produce and UP and DN error pulses. If reference signal is leading the feedback signal then UP signal will produce pulse, that is equal to the difference in phase of input signals. Else DN signal will produce a pulse. If there is no phase difference UP and DN signals are zero. The design of PFD should be such a way that, there should not be dead zone (small change in phase of two signals that cannot be detected by PFD). Figure 2.3(a) represents no dead zone 2.3(b) represents non zero dead zone. The conventional PFD will suffer from high frequency of operation, non zero dead zone and with high power consumption.

III. DEIGN OF PHASE FREQUENCY DETECTOR



a)



b)

Fig .3.(a) Modified schematic of DFF for high speed PFD. (b) Block diagram of complete PFD.

The design of PFD is done to completely remove reset path delay and it retains the properties of phase frequency detector. This design works fine with any difference in phase, enables high frequency of operation and also provides fast lock time. The phase frequency detector finds the phase difference between CLKREF and CLKVCO and produces the outputs UP and DOWN. The both D flip flops shown in the figure 3(b) is identical. The smallest device sizes possibly drawn in 0.18um process to obtain a high speed PFD. The DFF consists of 9 transistors, so the PFD will be having total of 18 transistors. The design of this phase frequency detector ensures low power of operation with no dead zone. The DFF is enhanced to operate at high frequency, this ensures that PFD will be able to operate at high frequency. We analyzed transfer characteristics of different PFD topologies. The simulation and analysis has done for 3

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conditions of operation for PFD (1) When CLKREF is leading CLKVCO. (2) When CLKVCO is leading CLKREF. (3)When CLKREF and CLKVCO are equal. Figure 3.1 shows the schematic of phase frequency detector implemented in cadence.

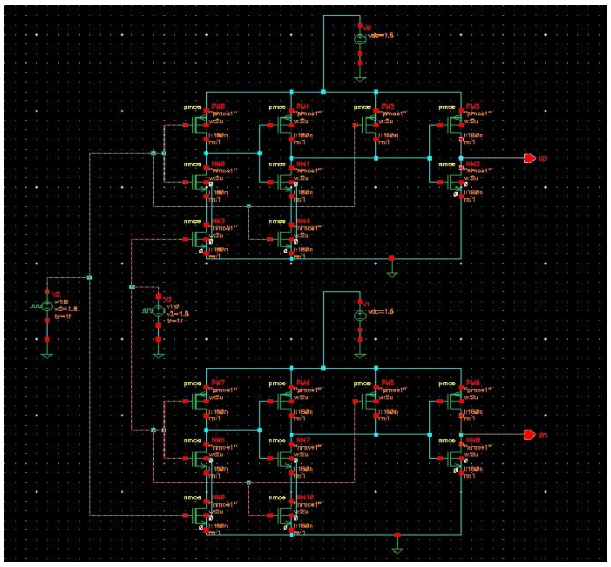

Fig 3.1.Design of phase frequency detector in cadence

IV. RESULTS AND DISCUSSION

The designed phase frequency detector is simulated in cadence virtuoso environment using CMOS 180nm process technology. The circuit is simulated with power supply of
1.8V. The small spikes at dead zone are found, but they are very small approximately equal to zero, with less pulse width. The average power of the PFD was found to be 42.7uw when operated at 400MHz reference frequency, which is least compared to the other designs implemented earlier. The PFD can be operated from 50MHz to 4GHz of reference signal. Figure 4(a), 4(b), 4(c) shows the simulation result of the PFD. In figure 4(a) we can see that output of the phase detector is approximately zero ,this is when inputs are equal there will be small spikes at dead zone with very less amplitude of 40mV peak to peak which is almost equal to zero. It has got small dead zone of 2ps. In figure 4(b), we can see that CLKREF is leading the CLKVCO so UP signal will produce a pulse and DOWN signal will be equal to zero. In figure 4(c), we can see that CLKVCO is leading the CLKREF, thereby PFD will produce DOWN signal and UP signal will be zero. In the simulation reference clock used is of 400MHz. Table 1 shows the comparison of various parameters of designed phase frequency detector with existing designs. The table will show that the designed PFD will be the optimized design. The design gives more flexibility for the researcher to design according to the application needs. Dynamic flip-flop will contribute to low power and low area. The drawbacks of the conventional phase frequency detector can be overcome by using the
circuit which is presented in this paper. The design satisfies the demand of digital circuit design and benefitting a modern operating system running at high frequency.

Figure

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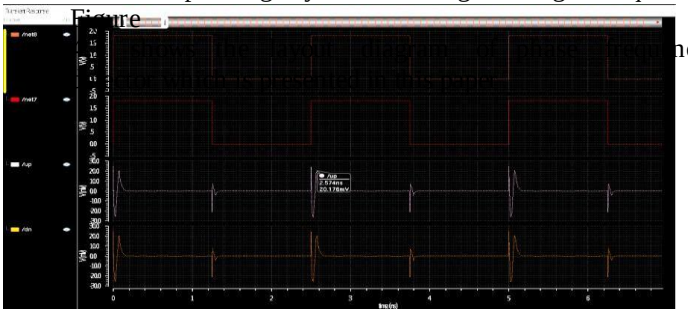
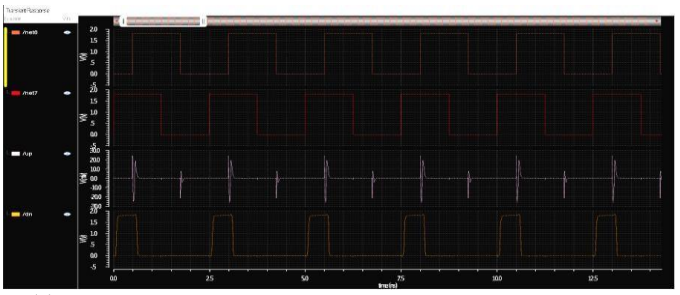


(a)

(b)



(c)

Fig. 4.Phase frequency detector outputs

CONCLUSION

Phase frequency detector is implemented in cadence virtuoso platform using CMOS 180nm process technology. The design has got 18 transistors which is operated at 1.8V power supply. The design has got very less dead zone of 2ps and it has got low power consumption of 42.7uW. This design maintains circuit stability when operated at both low and very high frequency

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