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Design of Low Power and High Speed 4-Bit Ripple Carry Adder Using GDI Multiplexer

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***Abstract*—The low power and less delay ripple carry adder has been proposed in this paper. On the base of GDI multiplexer, 12T full adder is designed. First the architecture of 28T full adder and**
12T full adder has been designed. Gate Diffusion Input (GDI) is a current approach in decreasing delay, power consumption and area of digital circuits. Here the performance comparison between 28T based ripple carry adder and 12T based ripple carry adder is presented. Both the designs has been developed and compared. The analysis shows that the 12T GDI based ripple carry adder is better than 28T based ripple carry adder. This work compares the performance of both ripple carry adders in terms of power and delay using 180nm technology.

***Index Terms*— Low power, Gate Diffusion Input, Transistor, Transistor.**

I.INTRODUCTION

The development of nanotechnology, with the enormous advancement of contemporary electronic system and also the low power & high speed devices are at the lead. Because of growing technology in recent years, speed and portability are the important parameters to be concerned. It needs high throughput, less power consumption and small sized circuitry. Pass transistor logic techniques are being used to design a logic circuits. Many different techniques have been introduced to get favorable results in speed and power consumption. In 2002, a new technique called Gate Diffusion Input was proposed by Israel A. Wagner, A. Fish, A. Morgenshtein.

The main intention of this work is to design a12T GDI based full adder and to compare the 28T based ripple carry adder and 12T based ripple carry adder. The purpose of this design is, on using the less transistors the delay and power gets reduced when compared between 12T and 28T ripple carry adders. Low power adders having the capability of reducing the power , delay and layout area. A circuit with cascaded N-bit full adder called ripple carry adder. The rippling of carry bit takes place in the ripple carry adder. It is so simple circuit hence it allows a fast design time. The first least significant adder in the ripple carry will be always a half adder.

II.FULL ADDDER

Boolean expressions which defines the sum and carry

Sum =A^B^C -----equation.1
Carry=AB+BC+CA-------equation.2

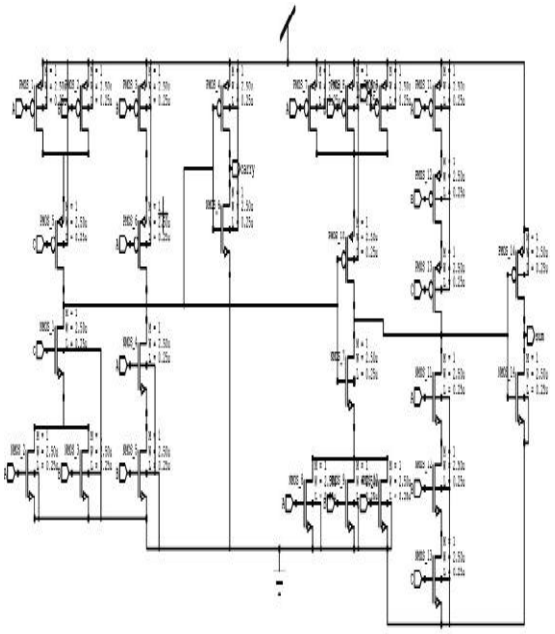

Fig.1 28T 1-bit full adder

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III. GATE DIFFUSION INPUT

Gate Diffusion Input is a new technique which produces a basic functions with two simple CMOS transistors. By using this GDI cell can reduce the area, delay and power in any circuit. GDI cell have one PMOS and one NMOS. It looks same like a inverter but the main difference is that inverter consists of one input but in this GDI cell it contains three inputs. In place of source nodes instead of sources the input pins are connected in this cell and both the gates of transistor are shorted then given to the input pin. The three inputs are P,N,G and output is D which shown in below fig.2.

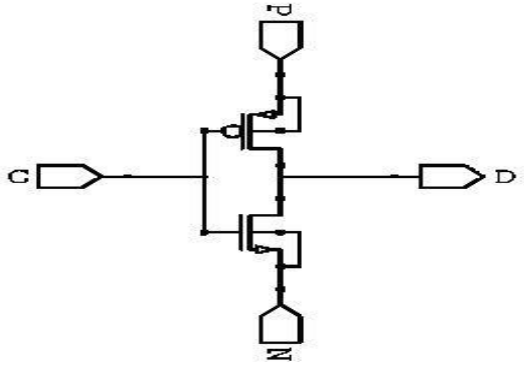

Fig.2. GDI cell

IV. ARCHITECTURE OF 12T FULL ADDDER Using

GDI technique the 2:1 MUX architecture has been implemented with the 2T (transistors). In the 2:1 MUX design the source of PMOS is connected to input pin 'B' in place of VDD and at the NMOS in place of VSS the input pin 'C' is connected. Both the gates of transistors are shorted and taken it as input select line 'A' which is shown in fig.3.

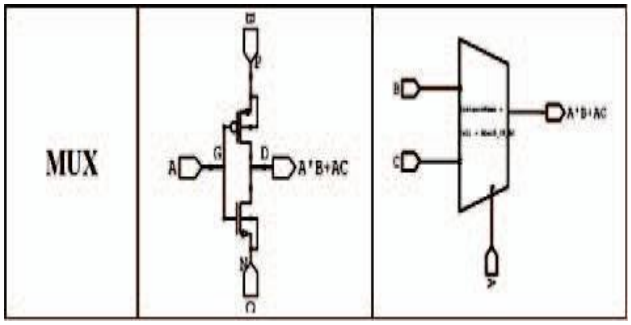

Fig.3. 2:1 MUX using GDI technique

PMOS operates for the low input and NMOS operates for the high input. The select line 'A' is low then value of input 'B' at the output and the select line is high, output is value of 'C'. This way of output resembles the 2:1 MUX.

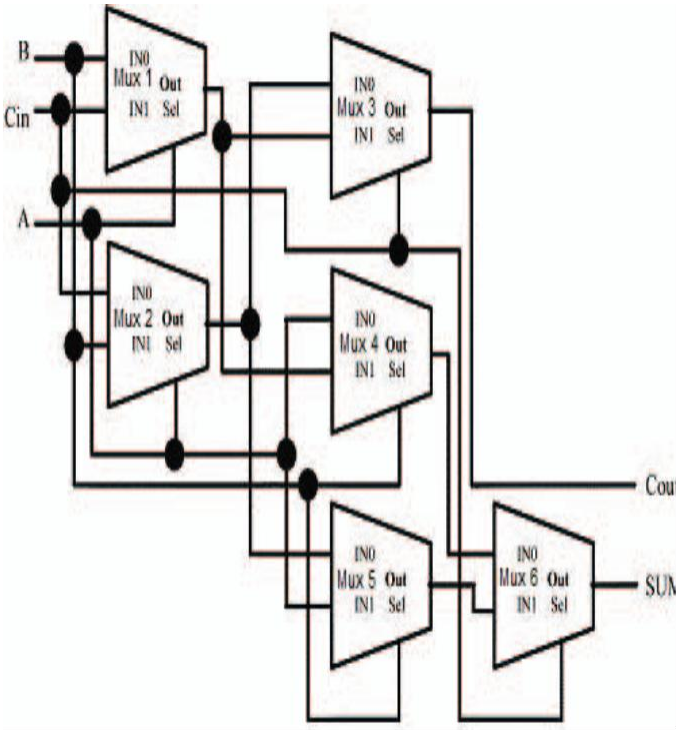

Fig.4. Block diagram of low power 12T full adder

By considering the 2:1 MUX here we designed the low power 12T full adder. It consists 6 number of 2T MUX which is shown in above fig.4. Every MUX in the above circuit have the same functionality. Below truth table shows the outcome of each 2T MUX.

TABLE.I. TRUTH TABLE FOR LOW POWER 12T FULL ADDER

A	B	Cin	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	SUM	Cout
0	0	0	0(B)	0(Cin)	0(Cin)	0(A)	0(Cin)	0(A)	0(A)	0(Cin)
0	0	1	0(B)	1(Cin)	0(B)	0(A)	1(Cin)	1(Cin)	1(Cin)	0(B)
0	1	0	1(B)	0(Cin)	0(Cin)	1(B)	0(A)	1(B)	1(B)	0(Cin)
0	1	1	1(B)	1(Cin)	1(B)	1(B)	0(A)	0(A)	0(A)	1(B)
1	0	0	0(Cin)	0(B)	0(B)	1(A)	0(B)	1(A)	1(A)	0(B)
1	0	1	1(Cin)	0(B)	1(Cin)	1(A)	0(B)	0(B)	0(B)	1(Cin)
1	1	0	0(Cin)	1(B)	1(B)	0(Cin)	1(A)	0(Cin)	0(Cin)	1(B)
1	1	1	1(Cin)	1(B)	1(Cin)	1(Cin)	1(A)	1(A)	1(A)	1(Cin)

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V. LOGIC ANALYSIS

The outcome of each 2T MUX is represented using Boolean functions. In order to get the sum and carry each 2T MUX is analyzed.

$MUX1 = (B\bar{A}+CA)$

$MUX2 = (C\bar{A}+BA)$

$MUX3 = [(C\bar{A}+BA)\bar{C}+(B\bar{A}+CA)C]$

$= AB\bar{C}+\bar{A}BC+AC$

$= AB\bar{C}+\bar{A}BC+AC(B+\bar{B})$

$= AB\bar{C}+\bar{A}BC+ABC+A\bar{B}C$

$= AB\bar{C}+ABC+\bar{A}BC+ABC+A\bar{B}C+ABC$

$= AB(C+\bar{C})+BC(A+\bar{A})+AC(B+\bar{B})$

$= AB+BC+CA = Cout$

$MUX4 = \bar{A}\bar{B}+(\bar{A}B+AC)B$

$MUX5 = (C\bar{A}+BA)\bar{B}+AB$

$MUX6 = [\bar{A}\bar{B}+(\bar{A}B+AC)B]\bar{C}+[(C\bar{A}+BA)\bar{B}+AB]C$

$= A\bar{B}\bar{C}+\bar{A}B\bar{C}+\bar{A}\bar{B}C+ABC = A \oplus B \oplus C = Sum$

The main source of power dissipation is a short circuit current. When the PMOS and NMOS are ON then there will be a direct path from source to ground hence the power consumption rises during transition level. The 12T low power full adder will not find a direct path between source to ground hence less possibility for the short circuit current. And the power consumption is relatively low. As all the G nodes in the circuit are directly connected to inputs so there will be high speed transition at the output signal which means a less delay. Finally it gives outputs with lesser delay and with low power consumption.

VI.RIPPLE CARRY ADDER

The four 1-bit full adder circuits are linked or cascaded together to get 4-bit ripple carry adder. 28T full adder and 12T full adder are cascaded separately to analyze the delay and power consumption of both ripple carry adders. Every adder in the circuit having sum and carry outputs. The input is from the right side of a circuit because the first right block traditionally defines the least significant bit(LSB).

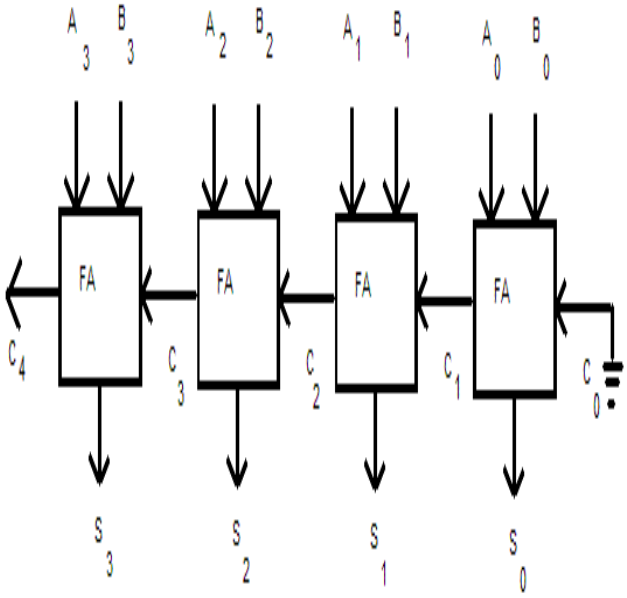

Fig.5. Circuit design of 4-bit ripple carry adder

VII. SIMULATION AND RESULTS

Simulation is used to analyze the circuit designs. Using standard simulator 180nm technology the 28T full adder & 12T full adder circuits are analyzed. Cascading of 28T and 12T full adders which makes 4-bit ripple carry adder to simulate and compare the performance analysis. The input parameters in schematic editor shown in table II.

TABLE.II. INPUT SPECIFICATIONS FOR 180NM TECHNOLOGY SIMULATION

Source Type	Bit
Zero Value	0 V
One Value	2 V
Bit ON Time and OFF Time	10ns
Rise Time	1ns
Fall Time	1ns
Bit Parameter (Input A)	00001111
Bit Parameter (Input B)	00110011
Bit Parameter (Input C)	01010101
Simulation Stop Time	80ns

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The schematic diagrams of 28T full adder and low power 12T full adder are shown in fig.6 & 7.

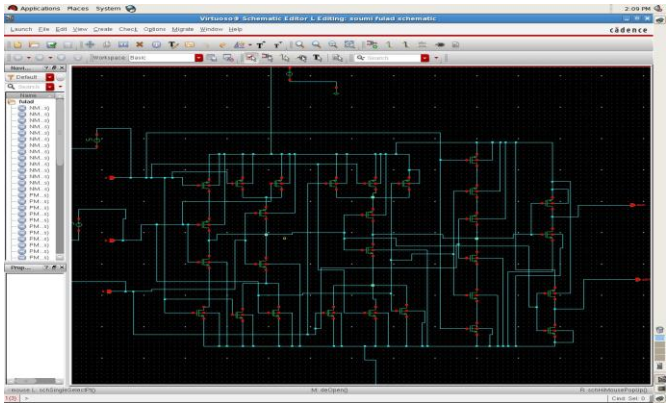

Fig.6. Schematic of 28T full adder

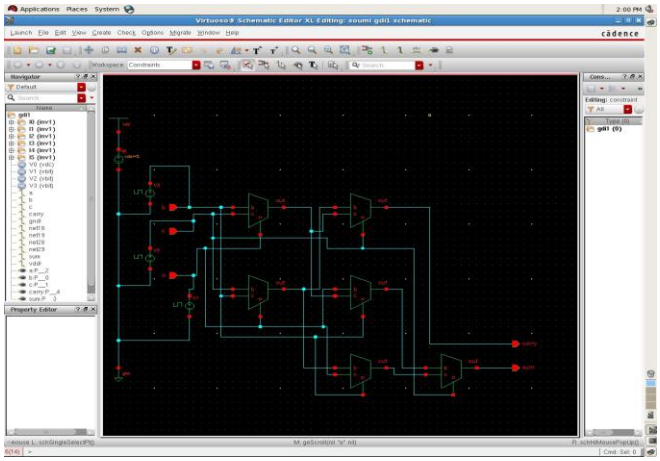

Fig.7. Schematic of low power 12T full adder

The schematic diagrams of cascaded 28T full adder and cascaded low power 12T full adder are shown in fig.8 and 9.

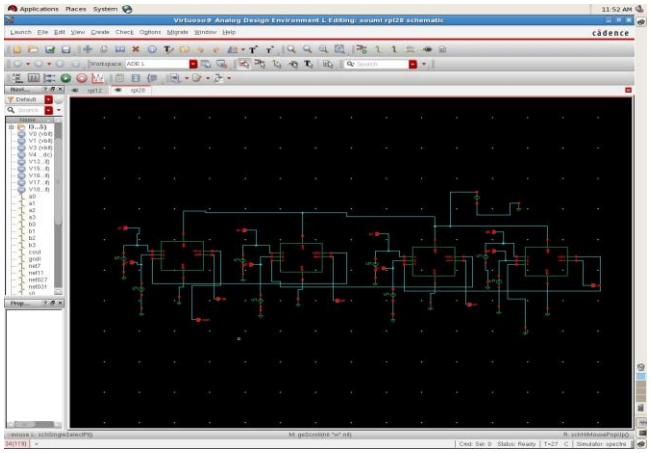

Fig.8. Schematic of 28T based ripple carry adder

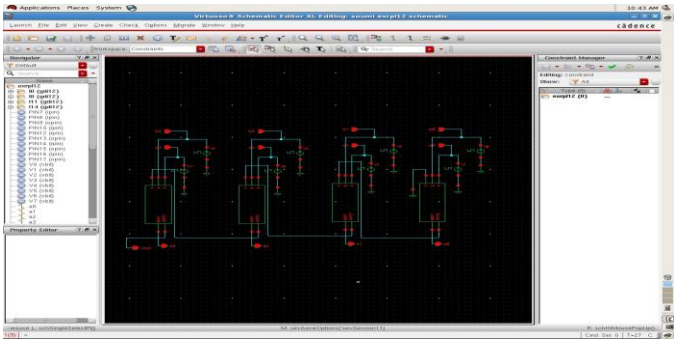

Fig.9. Schematic of 12T based ripple carry adder

The transient responses of adder schematics when they are simulated are given below

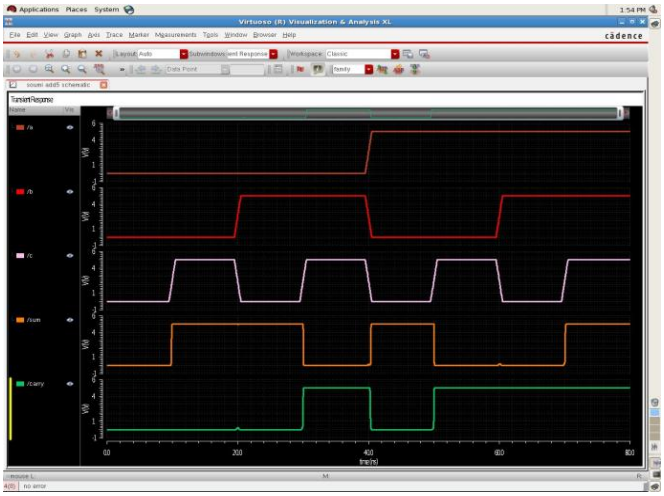

Fig.10. Transient response of 28T full adder

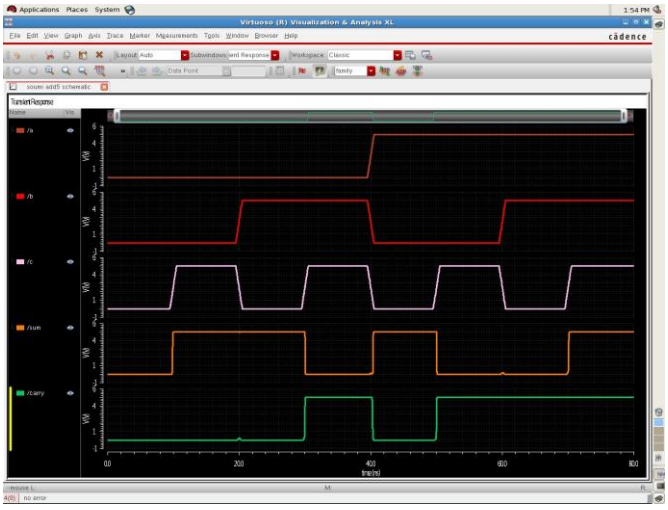

Fig.11. Transient response of 12T full adder

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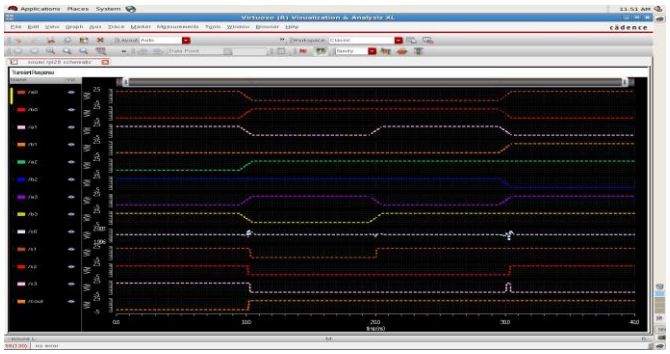

Fig.12. Transient response of 28T based ripple carry adder

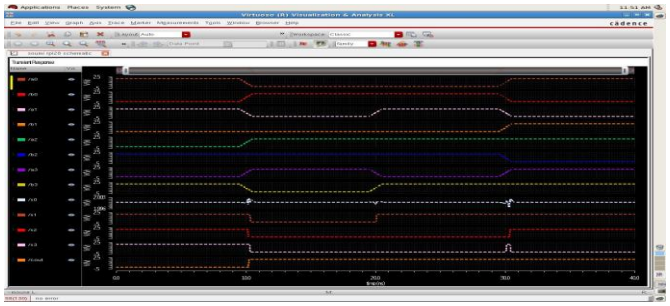

Fig.13. Transient response of 12T based ripple carry adder

From Fig 12 and 13 states that 12T based ripple carry adder having the same transient response as 28T based ripple carry adder. The power and delay analysis comparison is given in the table III.

TABLE.III. COMPARISION BETWEEN 28T BASED AND
12T BASED RIPPLE CARRY ADDER

	28T BASED 4-BIT RIPPLE CARRY ADDER	12T BASED 4-BIT RIPPLE CARRY ADDER
Average power analysis	46.05 uw	5.453 uw
Delay analysis	209.5 ps	81.5 ps

VIII.CONCLUSION

In this paper the results concludes that 12T based ripple carry adder has got better performance in comparison with
28T based ripple carry adder on consideration of power and delay.
Even it shows that on using the 2T MUX GDI technique can reduce the area of a full adder.

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