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DESIGN OF FINFET

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Abstract -- Since the fabrication of MOSFET, the minimum channel length has been shrinking continuously. As devices shrink further and further, the problems with conventional (planar) MOSFETs are increasing. Industry is currently at the 90nm node (i.e., DRAM half metal pitch, which corresponds to gate lengths of about 70nm). As we go down to the 65nm, 45nm, 32NM, 22nm, 14nm etc., nodes, there seem to be no viable options of continuing forth with the conventional MOSFET. The motivation behind this decrease has been an increasing interest in high speed devices and in very large scale integrated circuits. The sustained scaling of conventional bulk device requires innovations to circumvent the barriers of fundamental physics constraining the conventional MOSFET device structure.

I. INTRODUCTION

Alternative device structures based on **silicon-on-insulator (SOI)** technology have emerged as an effective means of extending MOS scaling beyond bulk limits for mainstream high-performance or low-power applications. **Partially depleted (PD) SOI** was the first SOI technology introduced for high-performance microprocessor applications. The **ultra-thin-body fully depleted (FD) SOI** and the **non-planar FinFET** device structures promise to be the potential "future" technology/device choices.

Here, we review the design challenges of these emerging technologies with particular emphasis on the implications and impacts of individual device scaling elements and unique device structures on the circuit design. The term "FINFET" describes a non-planar, double gate transistor built on an SOI substrate, based on the single gate transistor design the important characteristics of FINFET is that the conducting channel is wrapped by a thin Si "fin", which forms the body of the device. The thickness of the fin determines the effective channel length of the device.

II. LITERATURE SURVEY

FINFET is a transistor design first developed by Chenming Hu and his colleagues at the University of California at Berkeley, which tries to overcome the worst types of SCE(Short Channel Effect).Originally, FINFET was developed for use on Silicon-On-Insulator(SOI). SOI FINFET with thick oxide on top of fin are called "Double-Gate" and those with thin oxide on top as well as on sides are called "Triple-Gate" FINFETs [7].

III. DESCRIPTION ABOUT FINFET

Type 3 DG-FETs are called FinFETs. Even though current conduction is in the plane of the wafer, it is not strictly a planar device. Rather, it is referred to as a quasi-planar device [13], because its geometry in the vertical direction (viz. the fin height) also affects device behavior. Amongst the DG-FET types, the FinFET is the easiest one to fabricate [3]. Its schematic is shown in Fig.1. While the gate length L of a FinFET is in the same sense as that in a conventional planar FET, the device width W is quite different. W is defined as: $W = 2H_{fin} + T_{fin}$

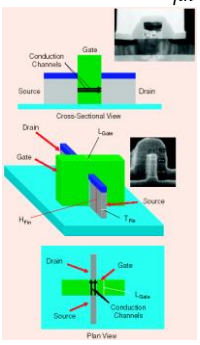

Fig 1: cross sectional view and plan view of FinFET

Where H_{fin} and T_{fin} are the fin height and thickness respectively and known as fin width. Because of the vertically thin channel structure, it is referred to as a fin because it resembles a fish's fin hence the name FinFET. A gate can also be fabricated at the top of the fin, in which case it is a triple gate FET. Or

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optionally, the oxide above the fin can be made thick enough so that the gate above the fin is as good as not being present [22].

IV. REASON FOR EVOLUTION

For the double gate SOI MOSFETs, the gates control the energy barrier between the source and drain effectively. Therefore, the Short Channel Effect (SCE) can be suppressed without increasing the channel impurity concentration [29].

V. GENERAL LAYOUT

The basic electrical layout and mode of operation of a FINFET does not differ from a traditional FET here is one source and one drain contact as well as a gate to control the current flow.

In contrast to planar MOSFET, the channel between source and drain is built as 3D bar on top of the Silicon subrstrate and are called fin [22].

VI. FINS

The fin is used to form the raised channel. As the channel is very thin the gate has a great control over carriers within it, but, when the device is switched on, the shape limits the current through it to a low level.

The thickness of the fin (measured in the direction from souce to drain) determines the effective length of the device.

VII. WHY FINFET IS USED?

Researchers are making progress in developing new types of transistors, called finFETs, which use a finlike structure instead of the conventional flat design, possibly enabling engineers to create faster and more compact circuits and computer chips. The fins are made not of silicon, but from a material called indium-gallium-arsenide, as shown in this illustration. In addition to making smaller transistors possible, finFETs also might conduct electrons at least five times faster than conventional silicon transistors, called MOSFETs, or metal-oxide-semiconductor field-effect transistors [22].

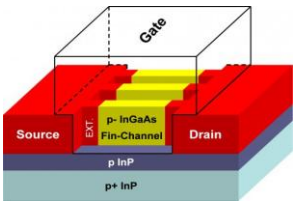

Fig 2: 3D view of FinFET

VIII. FINFET FABRICATION

The key challenges in FinFET fabrication are the thin, uniform fin and also in reducing the source-drain series resistance [7].

FinFET's have broadly been reported to have been fabricated in 2 ways:

Gate-first process: Here the gate stack is patterned/formed first, and then the source and drain regions are formed [8].

Gate-last process (also called replacement gate process): Here source and drain regions are formed first and then the gate is formed [9].

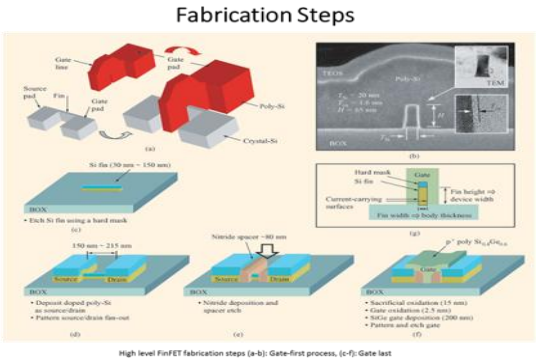

Fig 3: Fabrication process steps

FinFET's are usually fabricated on an SOI substrate. It starts by patterning and etching thin fins on the SOI wafer using a hard mask. The hard mask is retained throughout the process to protect the fin. The fin thickness is typically half or one third the gate length, so it is a very small dimension. It is made by either e-beam lithography or by optical lithography using extensive linewidth trimming [29].

In the gate-first process, fabrication steps after the fin formation are similar to that in a conventional bulk MOSFET process. In the gate-last process, the source/drain is formed immediately after fin patterning [30].

The heart of the FINFET is a thin Si fin, which serves as a body of the MOSFET.A heavily doped poly Si film wraps around the fin and makes the electrical contact to the vertical faces of the fin. A gap is etched through the poly Si film to separate the source and drain [24].

The various steps in the fabrication of FINFETs are discussed as follows.

A. CHEMICAL VAPOUR DEPOSITION (CVD)

- SiN and SiO layers are deposited on Si film to make a hard mask or a cover layer.

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- The cover layer will protect the Si fin throughout the fabrication process.
- Then, a layer of SiO2 is developed by the process of dry etching.
- The layer of SiO2 is used to relieve the stress [29].

B. ELECTRON BEAM LITHOGRAPHY

- The fine Si fin is patterned by EB Lithography with 100keV acceleration energy.
- The resist pattern is slightly ached at 5W and 30 sec to reduce the Si fin width.
- Then using top SiO layer as a hard etching mask, the SiO layer is etched.
- By this process, the silicon fin is patterned.
- A thin layer of sacrificial layer of SiO2 is grown.

Then, the sacrificial oxide is stripped completely to remove etch damage. While the cover layer protects the Si fin, the amorphous Si is completely removed from the side of the Si fin. The amorphous Si is in contact with the Si fin at its side surfaces becomes the impurity diffusion source that forms the transistor source and drain [29].

C. OXIDATION

The gate oxidation should thin the Si fin width slightly. By oxidizing the Si surface, gate oxide as thin as 2.5nm is grown. Because the area of Si fin inside the surface is too small, we use dummy wafers to measure the oxide thickness. Hence the gate oxide is grown [24].

D. FORMATION OF POLY-Si GATE

The boron doped Si is deposited at 475`C as the gate material. Because the source and drain extension is already formed and covered by thick SiO layer, no high temperature steps are required after the gate deposition. The total parasitic resistance due to probing is about 3000 [24].

E. HOW TO REDUCE COMPLEXITY OF FABRICATION???

Due to the complexity of fabrication process, the FINFET design was proposed to have a delta structure, so that after the reduction of vertical feature height, the gate channel-Gate stacked structure is realized by a Quasi-Planar technology [13].

IX. EVALUATION OF FINFET

- Current performance is poor.
- Conducted only in high voltages

X. REASON FOR POOR PERFORMANCE:

Large bits and holes in the Si fin and the source drain areas.

In fabrication, photo resist alone is not a sufficient task.

XI. PARASITIC CAPACITANCE

Parasitic capacitance is also known as stray capacitance. In electrical circuits, parasitic capacitance is an unavoidable and usually wanted capacitance that exists b/w parts of an electronic component or circuit simply because of their proximity (relationship) to each other.Circuit elements such as inductors, diodes and transistors have internal capacitance and derivate from the circuit elements [3].

XII. HOW TO AVOID PARASITIC CAPACITANCE

Additional process steps are required to induce impurities (appropriate type) below the fin to provide a Punch-Through Stop (PTS), ensuring there is no direct current path b/w gate and source and are electrically controlled by gate input [3].

XIII. SHORT CHANNEL EFFECT

It is an effect whereby a MOSFET in which the channel length is the same order of magnitude as the depletion layer widths of source & drain junctions, behaves differently from the other MOSFETs [3].As the channel length 'l' is reduced to increase both the operation speed and the number of components per chip, the so called SCE occurs [2].

TRI-GATE AND DUAL GATE FINFET

• A "hard mask" dielectric is retained on top of the fin.

• The electric field from the gate to the fin on the top is drastically reduced

XIV. ATTRIBUTES OF THE SHORT CHANNEL EFFECT

Limitation imposed on the electron drift characteristics in the channel. Modification of threshold voltage (Short Channel Effect (SCE))

FULLY DEPLETED FINFET (VOLUME) CHANNEL

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• The finFET channel is typically "fully depleted" by the gate voltage in the off state → little body effect (Vt dependency upon substrate bias).

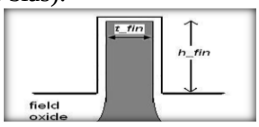

Fig 4: FinFET field oxide

Effective channel width (W)=(Tfin+(2*Hfin))
Effective channel length (Leff)=(Lgate+(2*Lext))

XV. RECENT DEVELOPMENT IN FinFET

Many developments are made in FinFET technology till date [1]. In order to fabricate a best possible FinFET with better performance, some factors were kept in mind. Series resistance should be low, as Ultra-thin fins result in better SCE [2], (but ultra-thin fins increased series resistance) .The fabrication process has to be easily integrate-able into conventional CMOS process to the extent possible. Keeping such considerations in mind and others, there have been many efforts to fabricate and characterize FinFETs. More recently, Kedzierski, fabricated a high performance FinFET using a *gate-first* process, with a 30nm gate length [23]. Epitaxial RSD, highly angled S/D implants, and $CoSi_2$ silicidation were used to reduce series resistance. High performance nFETs and pFETs with I_{ON} of 1460uA/um and 850uA/um were reported [19]. The fin thickness and height was 20nm and 65nm respectively, with a 1.6nm oxide [21]. Many devices were fabricated to specifically study the effect of fin thickness and height on the series resistance. Devices were fabricated in the <100> as well as <110> direction [9].

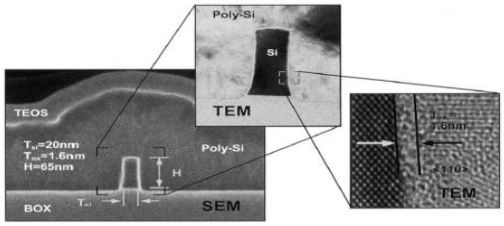

Fig 5: cross section of poly- sI of FinFET

XVI. ADVANTAGES OF FINFET

- Having excellent control of short channel effects in submicron regime and making transistors still scalable. Due to this reason, the small- length transistor can have a larger intrinsic gain compared to the bulk counterpart. Much Lower off-state current compared to bulk counterpart.
- Promising matching behavior.
- Low cost
- Higher technological maturity than planar DG.
- Suppressed Short Channel Effect(SCE)
- Better in driving current
- More compact

XVII. DISADVANTAGES OF FINFET

- Reduced mobility for electrons
- Higher source and drain resistances
- Poor reliability

XVIII. APPLICATIONS OF FinFET

DG devices like Fin FETs offer unique opportunities for microprocessor design. Compared to a planar process in the same technology node, FinFETs have reduced channel and gate leakage currents. This can lead to considerable power reductions when converting a planar design to fin FET technology [28]. Utilizing fin FETs would lead to a reduction in total power by a factor of two, without compromising performance [10]. Another possibility to save power arises when both gates can be controlled separately [12]. The second gate can be used to control the threshold voltage of the device, thereby allowing fast switching on one side and reduced leakage currents when circuits are idle. [30]

XIX. CONCLUSION

FinFETs are a necessary step in the evolution of semiconductors because conventional MOSFET has difficulties in scaling beyond 32 nm. Use of the Dual gate leads to very interesting design opportunities. Rich diversity of design styles, made possible by independent control of FinFET gates, can be used effectively to reduce total active power consumption. DG / TG MOS circuits provide an encouraging tradeoff between power and area

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