

# Design and Implementation of FM modem on FPGA for SDR using Simulink

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**Abstract - This paper describes the implementation of FM modulation and demodulation for Software Defined Radio (SDR). Due to high performance and reconfigurability, signal processing is done on FPGA. Analog modulation scheme like frequency modulation is performed in digital domain on virtex4 FPGA. Both transmitter and the receiver contain Direct Digital Synthesizer (DDS). DDS used to generate sinusoidal signals with Spurious Free Dynamic Range (SFDR) of 70DB. FM modem has been implemented by using Simulink in MATLAB R2012a. Feed-forward type of demodulation is used in the receiver by using CORDIC. DAC and ADC can be used for conversion of data from digital to analog and vice versa. DAC and ADC can be programmed in verilog by using SPI logic in Xilinx ISE. Implementation is done on VIRTEX4 FPGA with Xilinx ISE 14.7 System Generator.**

**Keywords- VIRTEX4 FPGA, SDR,FM modem, SFDR, CORDIC, Simulink.**

## 1. INTRODUCTION

Baseband signal processing technology is emerging as the major river. This technology has evolved towards the concept of software defined radios (SDR). In SDR the software will configure the hardware over the air according to the needs in the presence of different communication protocol. Main characteristic of SDR are their flexibility and reprogrammability. In SDR one can change the complete functionality just by replacing or modifying the software. This allows upgrading or improving the equipment without any modification in the hardware. Signal processing which is necessary to transmit and receive the baseband information can be done by

programmable digital design. Devices such as Digital Signal Processor (DSP) and Field Programmable Gate Array (FPGA) offers greater flexibility and potentially longer life, since the radio can be upgraded very cost efficiently with software. FPGA's gives less area, cost and higher performance. In an audio broadcasting excellent clarity of audio and voice is the main concern. VCO suffers from nonlinearity over the desired frequency range and hence its very difficult to obtain a good clarity in FM modulated and demodulated signal. This has floor the way for digital implementation of FM modulation and to replace analog implementation ensuring linearity over the entire frequency range, designer choose to replace the VCO by DDS (or NCO). DDS used to generate sinusoidal signals by employing lookup table scheme. Digital integrator in DDS used to map lookup table into sinusoidal waveforms. In order to process a signal we use frequency modulation and demodulation concept. Discriminating accurately a small frequency deviation of the modulated signal from its centre frequency is the basic fundamentals behind Fm demodulation. Feed-forward method is one of the popular techniques for FM demodulation. The feed=forward type of demodulation here is called ArcTan differentiator system, was based on an "unwrapper" four quadrant ArcTan. The ArcTan operation was realized by the Xilinx CORDIC ATAN block, which was implemented using basic building blocks from Xilinx blockset.

## 2. FM MODULATOR

FM Modulation technique is a technique where the frequency of the carrier signal is varied with respect to message signal. Modulation can be obtained by multiplying a message signal with a carrier signal. Frequency of modulating signal must be lower than the carrier.FM modulator contains an up converter,

DDS, adder. Up converter used to increase the number of samples for better performance. DDS takes the data and generate sinusoidal from the lookup table. Adder adds the instantaneous frequency of the message and carrier signal

$$s(t) = A_c \cos(\theta(t))$$

$$\theta(t) = 2\pi f_c t + 2\pi k_f \int m(t) dt$$

$$s(t) = A_c \cos[2\pi f_c t + 2\pi k_f \int m(t) dt]$$

### 3. FM DEMODULATOR

The message signal  $m(t)$  may be recovered from a FM modulated wave  $s(t)$  by multiplying  $s(t)$  with the carrier signal frequency as:

$$s(t) = A_c \cos[2\pi f_c t + 2\pi k_f \int m(t) dt]$$

$$p(t) = k_f \int m(t) dt$$

$$\text{in-phase} \Rightarrow s(t) * \cos(\omega_c t) \quad \text{quadrature-phase} \Rightarrow s(t) * \sin(\omega_c t)$$

$$\Rightarrow A_c/2 \sin(p(t)) \quad \Rightarrow A_c/2 \cos(p(t))$$

#### A. I and Q generator

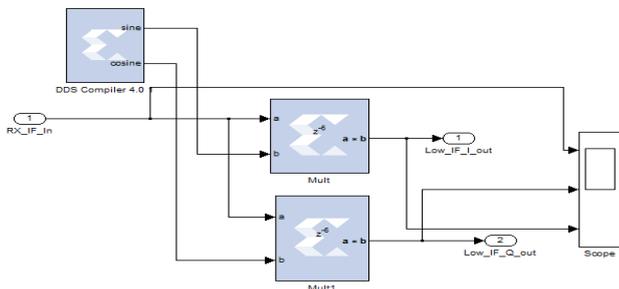


Fig1: I and Q generator

The signal which is received has the centered frequency of 10.7MHz. this signal can be digitized by using 14 bit ADC. The signal is multiplied by cosine wave to generate in-phase (I) signal and by sin to generate out-phase (Q) signal which is phased out by 90°.

#### B. DEMODULATOR

Demodulator used is feed-forward method of demodulator which is called as Arc Tan differentiator.

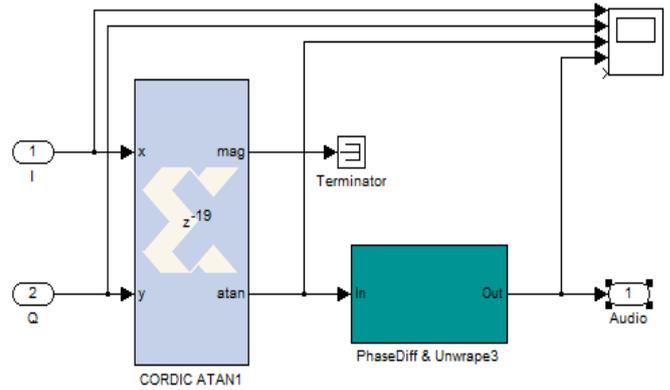


Fig2: Demodulator

Instantaneous frequency of the baseband signal is computed in demodulation part. We first calculate the phase angle of the signal then the derivative of phase angle will give the instantaneous frequency. Below are the expressions:

$$\Phi(t) = \text{Arc Tan}(Q/I) \text{-----(1)}$$

$$\text{Instantaneous frequency } [f(t)] = d\Phi / dt \text{-----(2)}$$

From the signal I and Q 8 MSB bits are taken to use them as the address of 64KB ROM. 8MSB of ROM corresponds to 8 MSB of signal I. 8 LSB of ROM corresponds to 8 MSB of signal Q. therefore the address of ROM is specified from the 8 MSB of I and Q signals. The content of the ROM is the value of ATAN (Q/I). The phase of the demodulated signals can be computed for every pair of (I, Q). Difference of ATAN is calculated to get the frequency  $f(t)$ . Xilinx CORDIC ATAN block realizes the arctangent operation and are implemented by using basic blocks in Xilinx blockset.

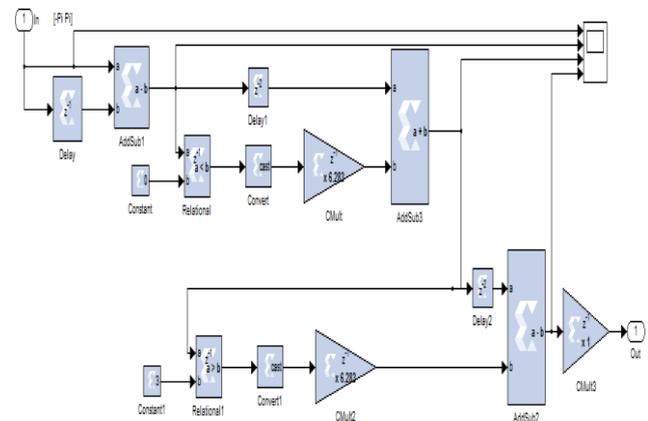


Fig3: phase diff and unwrap

#### 4. DAC CONFIGURATION

DAC5686 is the Digital to Analog Converter (DAC) to digitize the Analog signal that is received. DAC that we use is the 16 bit high speed DAC which has integrated interpolating filters, Numerically Controlled Oscillator (NCO), clock multiplier and the voltage reference. DAC has been specifically designed for low input data rates between DAC and FPGA , and it gives high frequency as the output. DAC configuration is done by using SPI logic. Serial peripheral interface (SPI) provides synchronous serial communication between master and slave devices. Spi have 3-wire and 4-wire configuration where in we use 3-wired SPI so that it reduces pin count and results higher throughput. It has MOSI and MISO lines combined to a single bidirectional data line which is called half duplex .

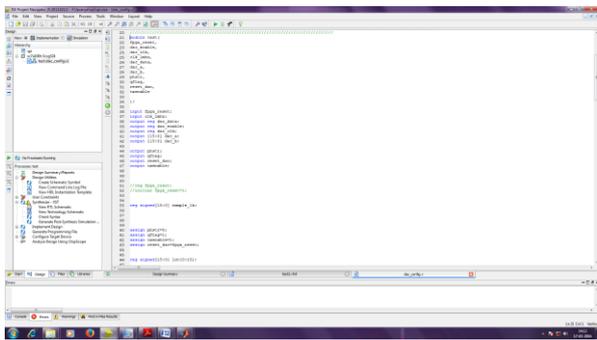


Fig4: DAC configuration in Xilinx

#### 5. PROPOSED FM MODULATOR

FM modulation is done as show in below figure. filters can be implemented in Xilinx CORE generator. Many types of filter r available like single rate, half band, Hilbert transform, we use single rate type of low pass filter to pass the signal below cut-off frequency. Then the signal is up sampled to increase the number of samples. DDS generates sine and cosine signals which are multiplied by carrier wave to produce modulated signal s (t).

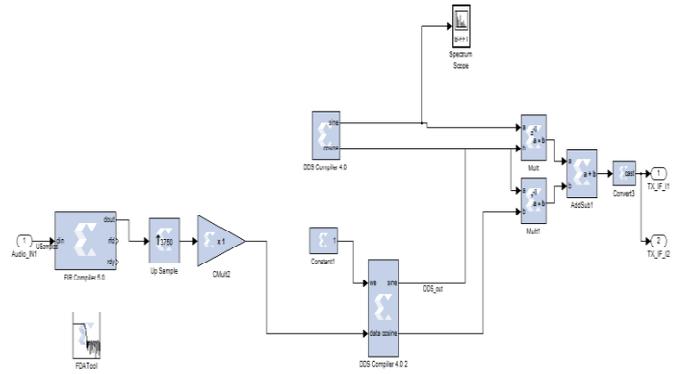


Fig 5. Proposed FM modulator

#### 6. PROPOSED FM DEMODULATOR

FM demodulation can be done by the method given in the below figure. The signal from the receiver is digitized by ADC the resultant signals is splitted into I and Q signals. From the values of I and Q ArcTan is computed in CORDEC followed by unwrapper to produce demodulated waveform.

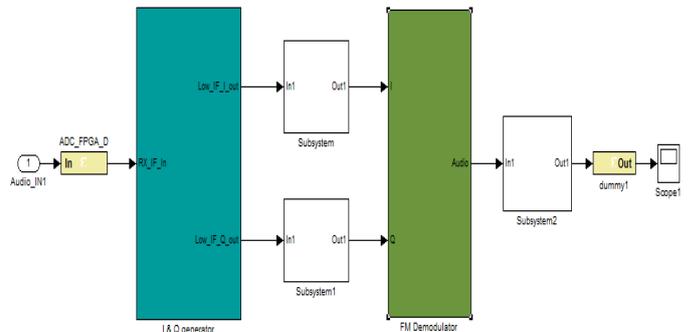


Fig 6. Proposed FM demodulator

#### 7. SIMULATION RESULTS

The DAC configuration is done by using Verilog HDL and Synthesized in Xilinx ISE platform.

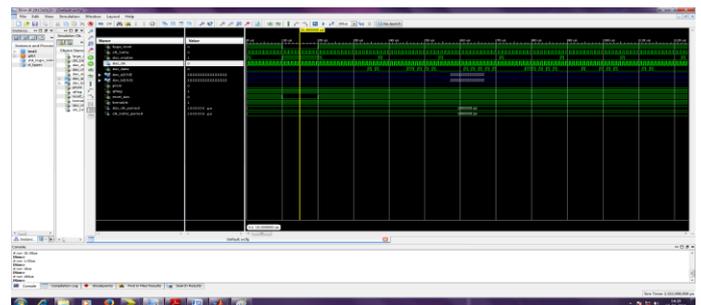


Fig7: output waveform of data transmission to DAC

FM modulated and demodulated signals are showed. The signal is a 1 KHz signal which is sampled at the rate of 16 KHz and the system frequency is 60MHz.

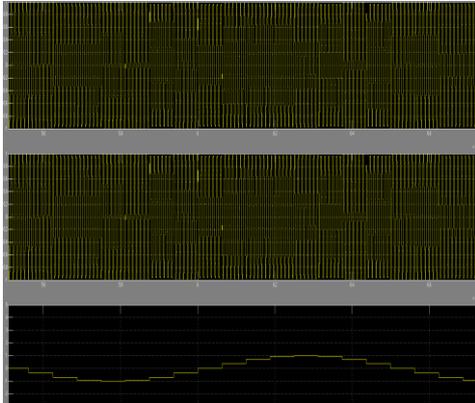


Fig 8. Simulation result of FM modulator

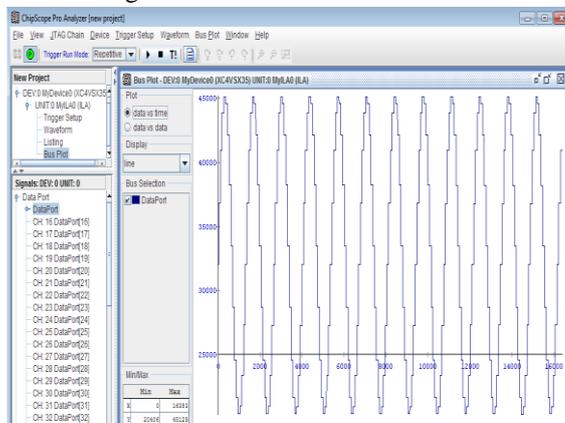


Fig9: simulation result of FM demodulator

## 8.CONCLUSION

The paper proposes design of FM modem using simulink and coding is done on Xilinx ISE. Implementation is done on virtex4 FPGA.

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