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Design and Implementation of reversible 8-bit ALU with optimized area, delay and power

Ms. CHAITHRA G,
M.Tech scholar,
School of Electronics and Communication Engineering,
REVA ITM, Bangalore, India.

Ms. NAYANA D.K.
Associate Professor
School of Electronics and Communication Engineering,
REVA ITM, Bangalore, India.

ABSTRACT

In digital signal processing, computer graphics, communication and cryptography Reversible or information-lossless circuits have gained better applications. Reversibility plays a prominent role when energy efficient estimates are considered. Reversible logic is used to minimize the power dissipation that occurs in conventional circuits by preventing the loss of data. This paper proposes a reversible design of an ALU. This ALU consists of eight operations, five logical operations and three arithmetic. The performed logical operations includes NOT, OR, AND, XOR and NAND and the arithmetical operations includes addition, multiplication, subtraction. All the modules are being designed using the basic reversible gates. The Area, power and delay analysis of the proposed module is achieved and a comparison with the conventional circuits is also carried out. We will design the ALU Design with the help of Verilog HDL and Simulated by Modelsim 6.4a Software. The Proposed ALU Design is synthesized by Xilinx and Implemented in to FPGA Spartan 3.

Keywords - ALU, reversible logic, submodules, area, delay, power.

I. Introduction

Computers now on the market are quicker, smaller and more multifaceted than their predecessors. However, the value paid for this speed and density is increased power consumption. The increase in clock frequency and the increased number of transistors packed onto a chip are the primary reasons for the rise in power consumption. In any digital processor, a group of 0s and 1s represents a number. Every process in a processor corresponds to the manipulation of the bits, e.g., flipping of 0 to 1 or 1 to 0.Internally, processors consist of millions of gates that perform logic operations. These logical operations in most cases, are so called irreversible. That is, some data about the inputs is deleted every time a logic operation (function) is performed. Thus, just by knowing the outputs alone, we cannot deduce the inputs. In addition, distinct logical states of a processor must be represented by distinct physical states of the computer hardware. Suppose that n bits are deleted (reset to zeros) due to irreversible logic operations. Before the erasure operation, these n bits could be in any of the 2n possible states. After the erasure, they are compressed to just one state. In order to compress the logical states of the processor, however, one must compress its physical states, thereby lowering the entropy of the hardware. By the Second Law of Thermodynamics, such decrease of entropy of the hardware leads to dissipated energy. As per R.Landauer's research, the amount of energy (heat) dissipated for every irreversible bit process is given by KT ln2, where K is the Boltzmann's constant (1.380×10-23 JK-1) and T is the operating temperature. For a room temperature T (300 K), KT ln2 is nearly 2.8×10-21 J, which is slight but non-negligible. If we assume that every transistor out of the 42 million(180 nm) transistors in a processor (e.g., Pentium IV) dissipates heat at a rate equivalent to its processor frequency(approximately 1 GHz), then its power consumption will be around $4.2\times1016\times KT$ ln2 = 0.052 Watt. However, according to Moore's law, the complexity, the speed, and hence, the heat dissipation due to the information loss will increase exponentially. If this existing trend continues, there will be an unbearable amount of heat generated by processor systems not so far down the road. Definitely, we need an alternative technologies that permit extremely low power consumption and heat dissipation in computing.

II. LITERATURE SURVEY

Reversible logic, which is an actively researching area, is considered as an apt alternative. The employ of reversible logical operations, which do not delete information, virtually dissipates "zero" heat. If the system would be able to return to its original state from its finishing state regardless of what occurred in between then no energy would dissipate from that system. This facilitates us to reproduce the inputs from the outputs. Reversible computing will make use physical mechanism that is logically as well as thermodynamically reversible. They are adiabatic systems that reprocess their energy and thus release very little heat. For a gate to be reversible, the logic function it comprehends has to be bijective. That is, there should be one-to-one mapping between the output and input vectors. These circuits can create exclusive output vector from each input vector, and vice versa.

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As per theory, each reversible gate has "dual" or "inverse". By connecting a reversible logic gate with its dual, we can run the logical operations backwards. This technology catches its application in wide range of areas which use extremely low power consumption.

III. concept of reversible logic gates

Reversible computation in a system can be implemented only when the system is composed of reversible gates. A circuit/gate is said to be reversible if the input vector can be separately recovered from the output vector and there is a one-to-one communication between its input and output assignments.

An N*N reversible gate can be denoted as

$Iv= (I1,I2,I3,I4,\ldots\ldots\ldots\ldots\ldots I_N)$

$Ov=(O1,O2,O3,\ldots\ldots\ldots\ldots\ldots O_N).$

Here, Iv and Ov represent the input and output vectors respectively. By considering the need of reversible gates in quantum computing, a literature survey has been done and the mostly available reversible logic gates are presented here.

1. BASIC DEFINITIONS

a. Reversible Function: The multiple output function *F*(*x1; x2; :::; xn*) of *n* Boolean variables is called reversible if:

i) The number of outputs is equivalent to the number of inputs;

ii) Any output pattern has a unique pre-image.

b. Reversible logic gate: Circuits in which number of outputs is equivalent to the number of inputs and there is a one to one correspondence between the input vectors and the output vectors are called Reversible gates.

c. Ancilla inputs/ constant inputs: This refers to the number of inputs that are said to maintain constant at either 0 or 1 in order to synthesize the given logical function.

d. Garbage outputs: To equalize the number of inputs and outputs, some additional inputs and outputs can be added. This refers to the number of outputs which are not used in the combination of a given function. In certain cases they are required to achieve reversibility.

Input + constant input = output + garbage.

e. Quantum cost: Quantum cost signifies the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of reversible logic gates (1*1 or 2*2) required to realize the circuit.

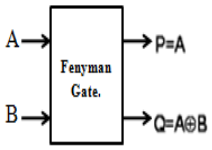
f. Flexibility: Flexibility refers to the absoluteness of a reversible logic gate in realizing more functions.

g. Gate Level: Gate level is the number of levels in the circuit which are required to realize the given logic functions.

2. REVERSIBLE LOGIC GATES

FEYNMAN GATE

The most familiar (2, 2) reversible gate is the **Feynman gate.** The Fig.2.1 shows the logical functions with input vector (A, B) and output vector (P,Q) performed by a Feynman gate and the truth table in table 2.1.



	A	B	P	Q
1	0	0	0	0
2	0	1	0	1
3	1	0	1	1
4	1	1	1	0

Fig 2.1:Feynman gate Table 2.1: Truth Table

One of the input bits in Feynman gate acts as control signal (A). That is, if A= 0 then the output Q follows the input B. If A = 1 then the input B is tossed at the output Q. So it is called as controlled NOT (1-NOT) and also called as quantum XOR because of its popularity in the field of quantum computing.

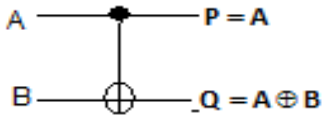
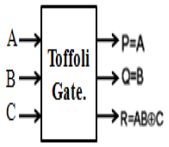


Fig 2.2: Circuit representation of Feynman gate

TOFFOLI GATE

The **Toffoli gate**, is a general reversible logic gate, which means that any reversible circuit can be constructed from Toffoli gates. It is also identified as the "controlled controlled not" gate, which describes its action. Toffoli gate is an example for (3, 3) reversible gates. Fig.2.3 shows the Toffoli gate.



	A	B	C	P	Q	R
1	0	0	0	0	0	0
2	0	0	1	0	0	1
3	0	1	0	0	1	0
4	0	1	1	0	1	1
5	1	0	0	1	0	0
6	1	0	1	1	0	1
7	1	1	0	1	1	1
8	1	1	1	1	1	0

Fig.2.3 Toffoli gate Table.2.2: Truth Table

When first two input bits are one, the third output bit is the inverse of third input bit i.e., A = B = 1, then R = C. When the third input bit is zero, Toffoli gate performs basic AND operation(C = 0; R = AB). As discussed earlier, any reversible gate has an inverse or dual.

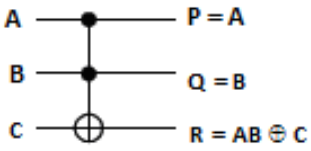


Fig.2.4: Circuit representation of Toffoli gate

FREDKIN GATE

Fredkin gate, shown in Fig.2.5, is a (3, 3) reversible gate .Here (A,B, C) represents the input vector and (P, Q, R) represents the output vector. Fredkin gate is also a self-reversible gate as it is its own inverse. It is a conservative gate because the hamming weight i.e., the number of logical ones of an input is same as its output. It uses 'A' as its control input: if A = 0, then the outputs simply replicates its inputs;

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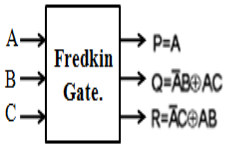
otherwise if A = 1, then the two input lines (B and C) is swapped at the output.



	A	B	C	P	Q	R
1	0	0	0	0	0	0
2	0	0	1	0	0	1
3	0	1	0	0	1	0
4	0	1	1	0	1	1
5	1	0	0	1	0	0
6	1	0	1	1	1	0
7	1	1	0	1	0	1
8	1	1	1	1	1	1

Fig.2.5: Fredkin gate Table.2.3: Truth Table

Fredkin gate is a universal gate, that is, by pre-setting some of its inputs in Fredkin gate we can construct the basic blocks such as AND, OR, NOT and other gate. It is universal, which intends that any logical or arithmetic operation can be constructed entirely of Fredkin gates. The Fredkin gate is the three-bit gate, if the first bit is 1, it swaps the last two bits.

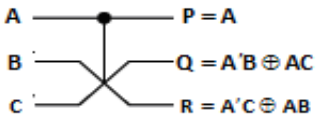


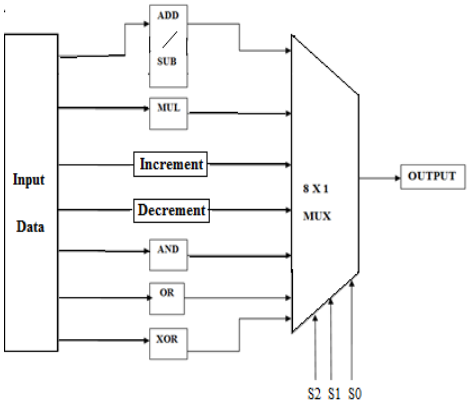
Fig.2.6: Circuit representation of Fredkin gate

The basic Fredkin gate is a controlled swap gate where the three inputs (C, I_1, I_2) are mapped onto three outputs (C, O_1, O_2). The input C is mapped directly to the output C. If C = 0, no swap will be performed; I_1 maps to O_1, and I_2 maps to O_2. Otherwise, I_1 will map onto O_2, and I_2 will map onto O_1 which means the two outputs are swapped. A simplified $n \times n$ Fredkin gate get ahead of its first n-2 inputs unchanged to the corresponding outputs, and if only when the first n-2 inputs are all 1 it swaps its last two outputs.

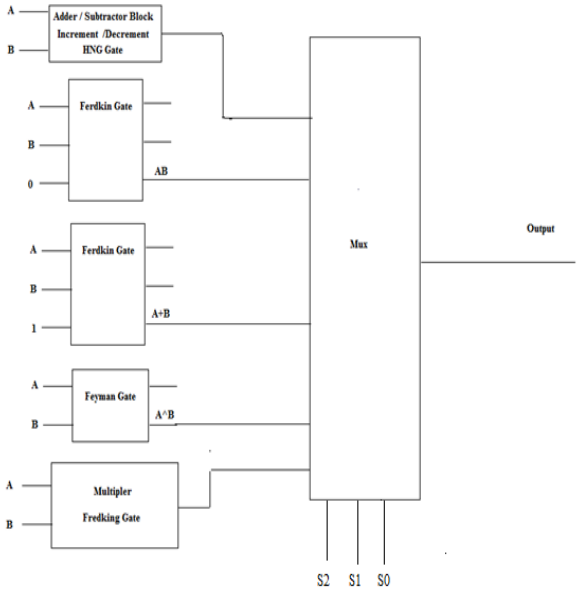
IV. DESIGN OF ARITHMETIC LOGIC UNIT

1. EXISTING CONVENTIONAL ALU DESIGN USED

The Arithmetic Logic Unit (ALU) is fundamentally part of a CPU. This allows the computer to accomplish basic arithmetical operation such as add, subtract, multiply, division and to perform basic logical operations such as AND, OR, increment etc. Every computer needs to be capable to do these simple functions, which are always included in a CPU.

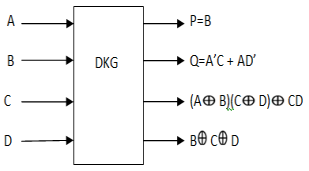


2. PROPOSED REVERSIBLE ALU DESIGN



REVERSIBLE ADDER:

The binary full adder/subtractor takes each input along with a carry in /borrow in that is produced as carry out/borrow out from the addition of preceding lower order bits. The n binary full adder/subtractor should be cascaded, if two n bit binary numbers are to be added or subtracted.



REVERSIBLE MULTIPLIER:

In a similar way n x n reversible multiplier can be designed using reversible TSG and Fredkin gates. However the full adder block is the basic cell for such a multiplier design. The TSG gate can be used as full adder when one of the inputs is assigned with a constant value of zero.

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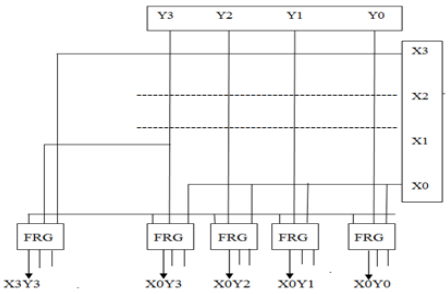
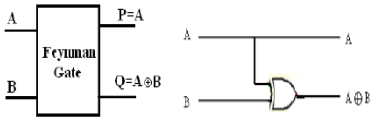


REVERSIBLE XOR:

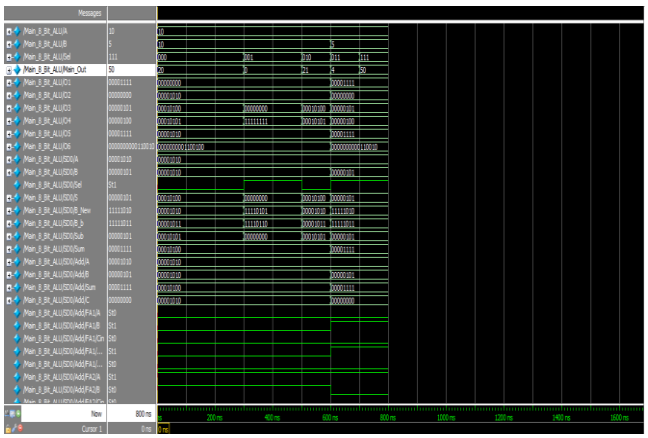
The 2*2 reversible Feynman gate having the input vector IN (A, B) and the output vector OUT (P, Q). The outputs are shown as P=A, Q=A XOR B



(a) Block diagram (b) Logic circuit

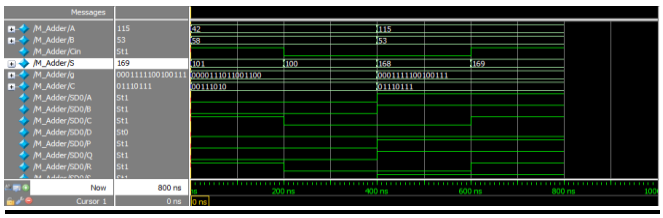
V. SIMULATION RESULTS

1. RESULT OF CONVENTIONAL ALU:

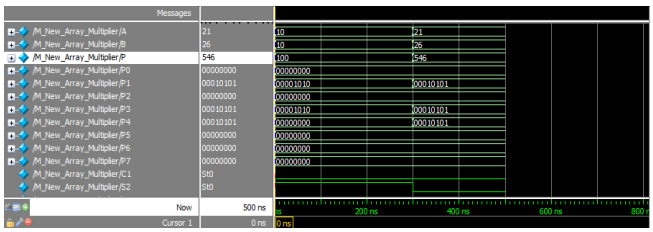


2. RESULTS OF PROPOSED ALU:

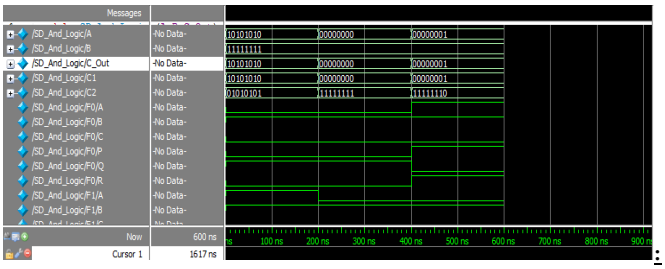
a. RESULT OF REVERSIBLE ADDER/SUBBTRACTOR:



b. RESULT OF REVERSIBLE MULTIPLIER:



c. RESULT OF REVERSIBLE LOGICAL OPERATION



3. AREA, DELAY and POWER COMPARISON:

METHOD NAME	AREA			DELAY			POWER
ALU NAME	LUT	GATE COUNT	SLICES	TOTAL	LOGIC DELAY	PATH DEALY	
CONVENTIONAL	136	873	72	26.71 ns	13.51 ns	13.2 ns	43mW
PROPOSED REVERSIBLE	120	759	65	24.62 ns	12.89 nS	11.73 nS	41mW

VI. CONCLUSION

The proposed 8 - bit reversible Arithmetic and logic unit is designed by adding adder/subtractor, multiplier and logical unit sub modules. The logical unit performs AND, OR, XOR. And arithmetic unit performs addition, subtraction and multiplication with increment and decrement operation depends on selected input bits. The performance correctness of the submodules are carried out using simulation tools and it was found that compare to conventional design, the proposed reversible logic showed a reduced area, power and delay in a considerable amount. As a **future work**, proposed design can be protracted to 16 – bit, 32 – bit and even for 64 – bits. Further divider block can also be included in ALU module. Moreover by combining proposed ALU with memory and other subsystems REVERSIBLE PROCESSOR design can be completed.

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Authors details:

1. Ms. CHAITHRA G.,M.Tech Scholar

Chaithra G is M.Tech scholar, School of Electronics and Communication Engineering, REVA ITM, Bangalore, India. She obtained her Bachelor degree in Electrical and Electronics Engineering, VTU, Karnataka, India in 2010. She is pursuing M.Tech in VLSI and Embedded system Visvesaraya technological University, Bangalore, Karnataka, India. Her research interest includes VLSI Design, analog VLSI and low power design.

2. Ms. NAYANA D.K. , Associate Professor

Prof. Nayana D. K. is working as Associate Professor, School of Electronics and Communication Engineering, REVA ITM, Bangalore, India. She obtained her Bachelor degree in Electronics and Communication Engineering from Mysore University, Karnataka, India in 1994 and Master of Technology degree in Digital Electronics and Advanced Communication from NITK, Surathkal, Karnataka, India in 1998. She is pursuing Ph. D. in Electronics and Communication Engineering, Jain University, Bangalore, Karnataka, India. She has more than 17 years of teaching experience. Her research interest includes VLSI Design and Digital Electronics.
Qualification: (Ph. D.), VLSI, awaiting for the final Viva-Voce. Jainu University, Karnataka, Indi M.Tech, Digital Electronics and Advanced Communication, NITK,Surathkal. B.E., Electronics and Communication Engineering, PESCE, Mandya (Mysore University)