International Journal of Engineering Research
Volume No.5 Issue: Special 5, pp: 992-1128
ISSN: 2319-6890)(online),2347-5013(print)
20 May 2016

DESIGN OF A BUCK CONVERTER

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***Abstract*— DC to DC converters are important in portable electronic devices. Such electronic devices often contain several sub-circuits, each with its own voltage level requirement than that supplied by the battery or an external supply (sometimes higher or lower than the supply voltage, and possibly even negative voltage). Switched DC – DC converters offer a method to convert one level of voltage to other, thereby saving space instead of using multiple batteries to accomplish the same thing. This work aims at designing a DC-DC Buck converter with input 28V and regulated 5V DC as output.**

Keywords: DC-DC converter, Buck converter.

I. INTRODUCTION

A. DC to DC converters are important in portable electronic devices such as cellular phones and laptop computers, telecommunication equipments, as well as DC motor drives which are supplied with power from batteries primarily.

The input to DC –DC converter is an unregulated DC voltage. The converter produces a regulated output voltage, having a magnitude (and possibly polarity) that differs from the input voltage. High efficiency is invariably required, since cooling of inefficient power converters is difficult and expensive. The ideal DC –DC converter exhibits 100% efficiency; in practice, efficiencies of 70%-95% are typically obtained. This is achieved using switched mode, or chopper circuits whose elements dissipate negligible power. Pulse width modulation (PWM allows control and regulation of the total output voltage). This approach is also employed in applications involving alternating current, including high efficiency DC–AC power converters (inverters and power amplifiers), AC AC power converters, and some AC-DC power converter (low harmonic rectifiers).

B. CLASSIFICATION:

NON-ISOLATING CONVERTERS:

- *Buck converter*- steps down the voltage.
- *Boost converter* –steps up the voltage.

Buck boost converter - The buck-boost can be used for either step down or step up.

ISOLATING CONVERTERS:

- *Fly back converter* - it operates like the buck-boost converter.
- *Forward converter* – Similar to fly back converter, but in contrast, there are two distinct phases for energy storage and delivery to the output, and the forward converter uses the transformer in a more traditional manner.

II. BUCK CONVERTER

The buck converter is used for voltage step down /reduction.

A. Basic Circuit

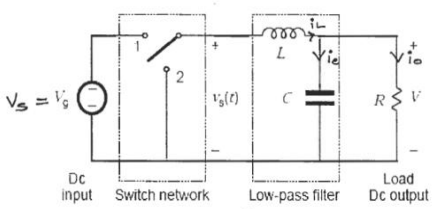

Fig1: Basic Circuit

The switch position is varied periodically, such that vs(t) is a rectangular waveform having period Ts and duty cycle. In practice, the SPDT switch is realized using semiconductor devices such as diodes, power MOSFETs, IGBTs, BJTs, or thyristors. The switch network changes the dc component of the voltage. By Fourier analysis, the dc component of a waveform is given by its average value. The average value of vs(t) is given by

$$V_s = \frac{1}{T_s}\int_0^{t_{on}} v_s(t)\,dt$$

$$= \left(\frac{t_{on}}{T_s}\right) \qquad V_g = DV_g$$

Since 0<D<1, the dc component of Vs is less than or equal to Vg.

ISSN: 2319-6890)(online),2347-5013(print)
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- *B. Realization of a Buck converter using MOSFET.*

Fig.2 illustrates one way to realize the switch network in the buck converter, using a power MOSFET and diode. A gate drive circuit switches the MOSFET between the conducting (on) and blocking (off) states, as commanded by a logic signal δ(t). When δ(t) is high (for 0<t<DTs), MOSFET Q1 conducts with negligible drain-to-source voltage. Hence, $v_s(t)$ is approximately equal to Vg, and the diode is reverse biased. The positive inductor current $i_L(t)$ flows through the MOSFET. At time t=DTs, δ(t) becomes low, commanding MOSFET Q1 to turn off. The inductor current must continue to flow; hence, $i_L(t)$ forward biases diode D1, and $v_s(t)$ is now approximately equal to zero. Provided that the inductor current $i_L(t)$ remains positive, diode D1 conducts for the remainder of the switching period. Diodes that operate in this manner are called freewheeling diodes. Since the converter output voltage v(t) is a function of the switch duty cycle D, a control system can be constructed that varies the duty cycle to cause the output voltage to follow a given reference v_r. Figure illustrates the block diagram of a simple converter feedback system. The output voltage is sensed using a voltage divider, and is compared with an accurate dc reference voltage v_r. The resulting error signal is passed through an op-amp compensation network. The analog voltage $v_c(t)$ is next fed into a pulse-width-modulator. The modulator produces a switched voltage waveform that is proportional to the control voltage $v_c(t)$. If this control system is well designed, then the duty cycle is automatically adjusted such that the converter output voltage v follows the reference voltage v_r, and is essentially independent of variations in vg or load current.

III. DESIGN

We have,

$\Delta I = V_a (V_s - V_a) / fLV_s$

$\Delta V_c = V_a(V_s - V_a) / 8LCf^2 V_s$

Initial conditions:

V_s=28V

V_a=5V

Ripple voltage=50mV

Ripple current=10% of output current

Output current=1A

Switching frequency=100 kHz

By substituting these values in the equations, we determine the values of L and C. We get, L=410µH and C=2.5µF.

Control circuit for buck converter is as shown in Fig.2

A. Principle of operation

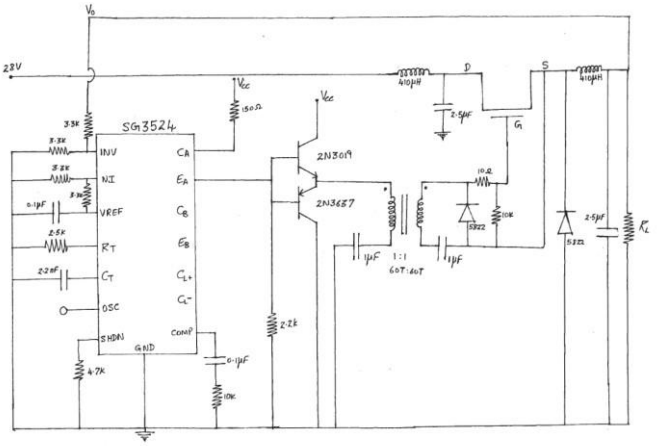

Fig.2: control circuit for buck converter

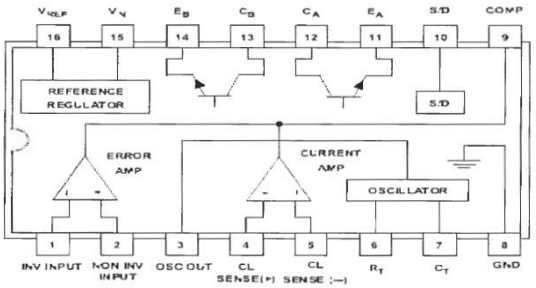

Fig.3: Pin diagram of SG3524

The SG3524 is a fixed-frequency pulse-width-modulation (PWM) voltage-regulator control circuit. The regulator operates at a fixed frequency that is programmed by one timing resistor, RT, and one timing capacitor, CT. RT establishes a constant charging current for CT. While this uses more current than a series connected RC, it provides a linear ramp voltage at CT which is used as a time dependent reference for the PWM comparator. The charging current is equal to 3.6V/RT, and should be restricted to between 30mA and 2mA. The equivalent range for RT is 1.8k to 100k. The range of values for CT also has limits, as the discharge time of CT determines the pulse width of the oscillator output pulse. The pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. A pulse width below 0.35us may cause failure of the internal flip flop to toggle. This restricts the minimum value of CT to 1000pF. (Note: Although the oscillator output is a convenient oscilloscope synchronous input, the probe capacitance will increase the pulse width and decrease the oscillator frequency slightly). Obviously, the upper limit to the pulse width is determined by the modulation range required in the power supply at the chosen switching frequency. Practical values of CT fall between 1000pF and 0.1pF, although successful 120 Hz oscillators have been implemented with values up to 5pF and a series surge limit resistor of 100 ohms. The oscillator frequency is

doi : 10.17950/ijer/v5i5/025

ISSN: 2319-6890)(online),2347-5013(print)
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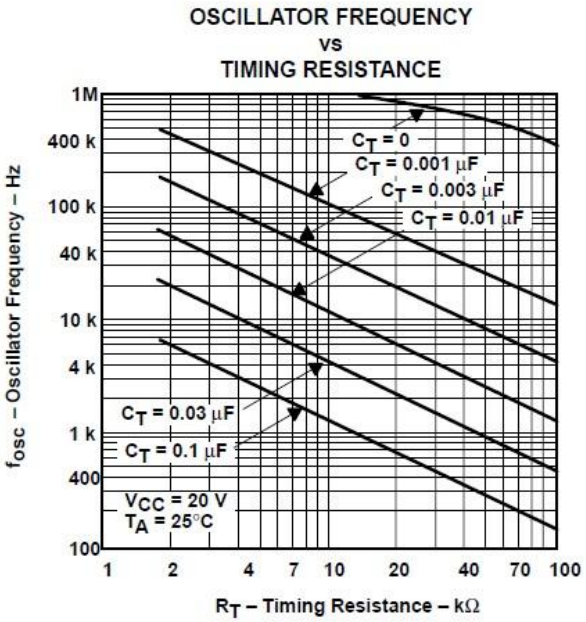
approximately 1/RT*CT; where R in ohms, C in µF and frequency is in MHz. Note that for buck regulator topologies, the two outputs can be wired for an effective 0- 90% duty cycle range. With this connection, the output frequency is the same as the oscillator frequency. For push-pull applications, the outputs are used separately; the flip- flop limits the duty cycle range at each output to 0-45%, and the effective switching frequency at the transformer is ½ the oscillator frequency. If it is desired to synchronize the SG3524 to an external clock, a positive pulse may be applied to the clock pin. The oscillator should be programmed with RT and CT values that cause it to free run at 90% of the external sync frequency. A sync pulse with a maximum logic zero of +0.3V and a minimum logic 1 of +2.4V applied to pin 3 will lock the oscillator to the external source. The minimum synchronous pulse width should be 200ns, and the maximum is determined by the required dead time. The clock pin should never be driven more negative than -0.3V, nor more positive than +5V. The nominal resistance to ground is 3.2k at the clock pin, ± 25% over temperature. If two or more SG3524 must be synchronized together, program one master unit with RT and CT for the desired frequency. Leave the RT pins on the slaves open, connect the CT pins to the CT of the master, and connect the clock pins to the clock pin of the master. Since CT is a high-impedance node, this synchronous technique works best when all devices are close together.

B. Estimation of RT and CT for the oscillating frequency of 200 kHz



IV.OBSERVATIONS

Output voltage Vo is observed for different values of input voltage Vi and load resistance RL and the values are tabulated.

RL=3.9kΩ **Vi=28V**

Vi (V)	Vo (V)
20	4.94
23.5	4.94
26.5	4.95
28	4.95
30	4.95

RL (kΩ)	Vo (V)
1	4.94
2.2	4.95
2.7	4.95
3.9	4.95

WAVEFORMS

1. Ramp waveform of CT at pin 7 of SG3524 with an oscillating frequency of 200 kHz.

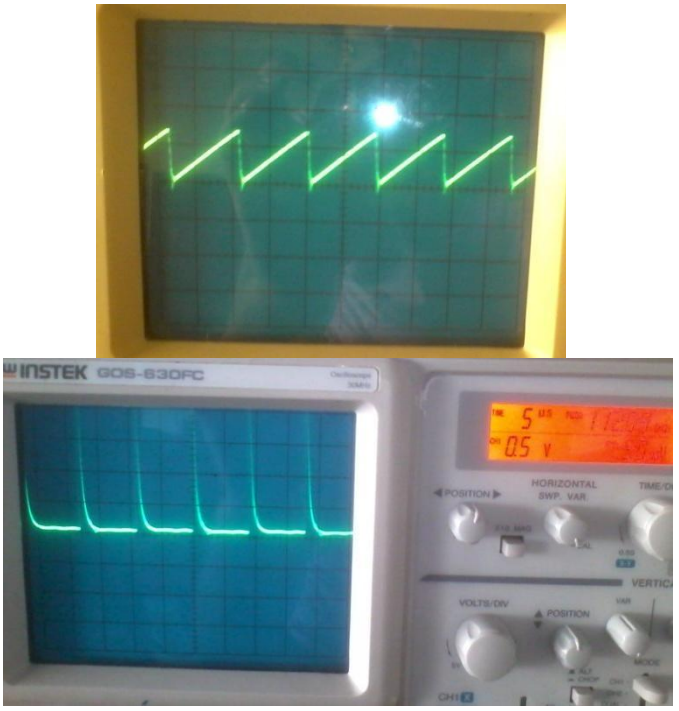


Fig.4. Waveform across output capacitor

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ISSN: 2319-6890)(online),2347-5013(print)
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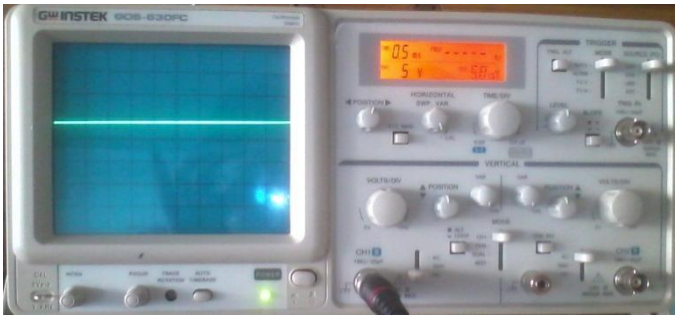

Fig.5. Regulated DC output

V. CONCLUSION

After obtaining experimental results, we see that DC output voltage of 5V stepped down from 28V, is obtained and the output is seen to be a regulated DC.

VI. ACKNOWLEDGEMENT

The authors would like to thank TEQIP II, MHRD and BMS College of Engineering for the financial support in the context of presented work.

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